Research on Typical Defect Electric Field and Temperature Characteristics of High Voltage Cable Terminal

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ABSTRACT During the installation of cable terminals, typical defects frequently occur due to construction practices. Defect types primarily include main insulation scratches, semiconductor tips, insulation layer impurities, and missing copper mesh. This study develops an electro-thermal coupled model to simulate and analyze the electric field and temperature profiles of terminals under typical defects. The results indicate that defects cause an increase in the electric field. Semiconductor tip defects increase the electric field strength by 6.72 times, causing the most serious electric field distortion. Main insulation scratches increase the electric field by 1.57 times, while insulation layer impurities increase it by 1.26 times. Additionally, missing copper mesh can also cause a slight increase in electric field strength. Simultaneously, defect size and location also influence the electric field strength field. More notably, the presence of defects will directly cause an increase in terminal temperature. The main insulation scratch caused a temperature increase of 1.94°C, the semiconductor tip caused a temperature increase of 1.6°C, the insulation layer impurity caused a temperature increase of 1°C, and the missing copper mesh caused a temperature increase of 8.7°C. When the ambient temperature rises, the defect temperature also increases accordingly.

INDEX TERMS cable terminal, insulation defect, electric field, temperature field, electrothermal coupling

I. INTRODUCTION

As urban areas expand, the deployment of high-voltage cables rated at 220kV and above has grown, accompanied by a gradual increase in their failure rate. Defects in cable terminals account for more than 39% of the operational failures in power cable lines [1]–[6]. During the installation of cable terminals, pushing the stress cone may leave scratches on the surface of the main insulation, causing surface damage and creating air gaps that lead to partial discharge. When stripping the semiconductive layer, operational errors can easily leave semiconductive tips on the main insulation. Poor sealing during terminal manufacturing may result in moisture ingress over long-term operation [7]–[10]. When defects exist in terminals, prolonged operation under high voltage and strong current environment can lead to insulation aging, which may cause explosions and fires. For example, In the process of installing a 220 kV cable terminal, improper operation left scratches on the surface of the main insulation. Electric field distortion occurred at the scratch locations, resulting in persistent partial discharge, insulation aging, and ultimately terminal breakdown [11]. In another case, a 220 kV cable terminal remained burrs and unevenness after insulation grinding. These imperfections introduced impurities at the contact surface where the stress cone meets the main insulation, initiating creeping electrical activity. Over time, this tracking penetrated completely, ultimately causing a cable terminal failure and explosion [12]. To prevent insulation accidents caused by partial discharges resulting from cable terminal defects, conducting simulation studies on the defect electric field and temperature field of terminals is crucial.

Regarding high-voltage cable electric field distribution research, literatures [13], [14] employed COMSOL Multiphysics simulation software to investigate the way electric field spreads in 320 kV DC cable joints. To investigate the electric field characteristics under specific defects, literature [15] utilized finite element simulation to analyze the effects of surface damage, main insulation scratches, and semiconductor layer air gaps on 110 kV cable intermediate joints. Literature [16] focused on cable terminations, employing finite element software to simulate electric field distributions when electrical impurities were located at different positions. Literature [17] analyzed the impact of silicone grease on the electric field profile of cable intermediate joints through ANSYS simulation software, and investigated the effect of silicone grease on impurity electric fields. Literature [18] analyzed the electric field distribution under different sizes of interfacial air gaps on the cable body and prefabricated components. Regarding the study of the temperature field in high-voltage cables, literature [19] used ANSYS software to analyze the temperature distribution characteristics when different defects exist in a cable intermediate joint. Literature [20] analyzed the influence of cable body length on joint temperature under different contact resistances of the intermediate joint. Literature [21] analyzed the temperature variation of the cable under common sheath faults. Literature [22] investigated the effects of ambient temperature, heat transfer coefficient, and material thermal conductivity on the temperature distribution of the terminal.

Numerous literatures have analyzed the electric field and temperature of cable accessories from different perspectives, providing a theoretical basis for actual terminal manufacturing and subsequent research on defect development mechanisms. However, these literatures have investigated the electric field and temperature independently. In practical engineering, the effects of electric fields and temperature on accessories are mutually coupled. Temperature increases cause changes in material parameters such as the tangent of the loss angle and dielectric constant, while the dielectric constant directly influences electric field distribution. Considering this coupling relationship more closely approximates actual operating conditions, thereby enhancing computational accuracy. Therefore, this study employs COMSOL Multiphysics software to perform electro-thermal coupling simulations on four common types of defects in high-voltage cable terminals. It aims to investigate the impact of each defect type on the terminal's electric field and temperature.

II. SIMULATION MODEL ESTABLISHMENT

A. CABLE PARAMETERS

The simulation employs a 220 kV single-core cable with a conductor size of 1,200 mm^2, whose specific structure is shown in FIGURE 1. The structural parameter settings for each section of the cable body in this study are shown in TABLE 1.

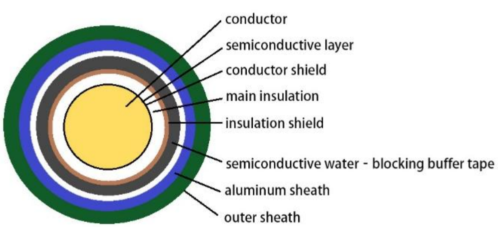


FIGURE 1. Power cable structure.

TABLE I. Units for Magnetic Properties

cable structure	thickness/mm	outer diameter/mm
conductor	–	42.6
semiconductive layer	0.3	43.2
conductor shield	1.5	46.2
main insulation	24	94.2
insulation shield	1.0	96.2
semiconductive water-blocking buffer tape	2	100.2
aluminum sheath	2.5	105.2
outer sheath	5.0	115.2

The structure of the cable terminal is shown in FIGURE 2. At the stress cone, the outer semiconductive layer is overwrapped with two layers of semiconductive tape, which are lapped with the base of the stress cone. Outside the semiconductive tape, a layer of grounding copper mesh s applied and grounded to the flange. This section sees the copper mesh attached to both the flange and the cable's outer layer, resulting in a zero-potential condition. The terminal tail is welded to the aluminum sheath via a lead seal, and the heat-shrink tube serves to protect the cable.

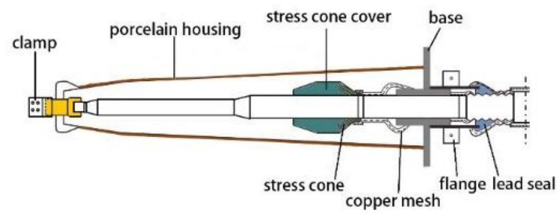


FIGURE 2. Cable terminal structure.

B. INFLUENCE OF FIBER TYPE ON PORE PRESSURE DEVELOPMENT: THEORETICAL STUDY

The behavior of electric current in the individual sections of the cable terminal follows Laplace equation. The governing equation is given as follows [23]:

$$\nabla \cdot (\gamma \nabla \varphi) = 0 \tag{1}$$

In the equation, φ represents the electric potential and γ represents the conductivity.

The primary internal heat sources inside the terminal consist of conductor loss, metallic loss, and dielectric loss from the insulation material [24]. Their respective calculation formulas are as follows:

$$W_c = I^2 R \tag{2}$$

$$W_s = \lambda_1 I^2 R \tag{3}$$

$$W_p = \omega C U^2 \operatorname{tg} \delta \tag{4}$$

In equation (2), Wc, I and R represent the Joule heating rate, current, and resistance of the conductor. In equation (3), Ws and $\lambda 1$ represent the induced Joule heating power and the metal loss factor. In equation (4), Wp, ω, C, U, and tanδ represent the dielectric loss generation rate, angular frequency, capacitance of the insulating material, voltage across the insulating material, and dissipation factor of dielectric materials.

Regarding loss in dielectric materials, since materials' permittivity varies with temperature, the term C in equation (4) can be derived from electric field calculations. Therefore, Equation (4) can be rewritten as [25]:

$$P = \omega C U \operatorname{tg}\delta \cdot \sum_{i=1}^{n} E_i S_i \qquad (5)$$

In equation (5), ε, Ei and Si represent the permitivity of the insulating material, field strength, and area. This expression serves as the numerical coupling calculation formula between temperature and electric field, enabling dynamic analysis.

In the simulation, cable core voltage, aluminum sheath, and current were set to 127 kV phase voltage, ground potential, 700 A. Temperature field employed solid heat transfer modeling with a heat transfer coefficient of 10 and an ambient temperature of 20°C. The electromagnetic-thermal multiphysics interface is selected.

C. SIMULATION MODEL

1) FLAWLESS

With reference to the actual cable terminals produced by the manufacturer, a 1:1 scale simulation model was established as shown in FIGURE 3. Material parameters across all components and assemblies are detailed in TABLE 2. Due to the symmetry of the cable terminal, a radial two-dimensional axisymmetric model is built along the central axis of the cable. At the copper shielding layer, the material parameters of the insulation self-adhesive tape and the heat-shrink tube are relatively close, and their influence on the electric field and temperature is minor. Therefore, during modeling, the self-adhesive tape is incorporated into the heat-shrink tube.

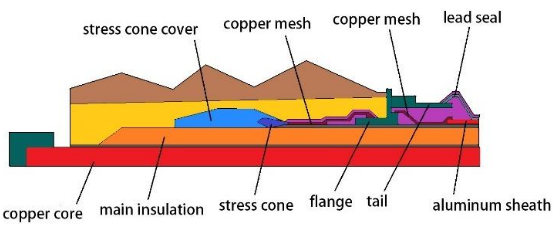


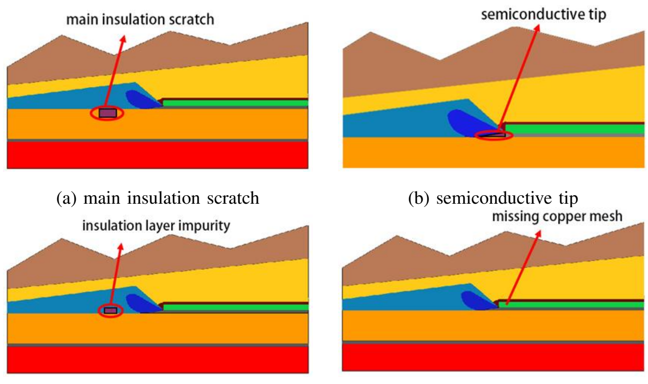
FIGURE 3. Model diagram of a cable terminal in normal operating condition.

TABLE II. Material simulation parameters

material	permittivity	thermal conductivity ($W{\cdot}K{\cdot}m^{-1}$)	electrical conductivity ($S{\cdot}m^{-1}$)
copper	10000	400	5.998×10^{7}
semiconductive material	30	0.1429	100
XLPE	2.25	0.2	7.3×10^{-14}
aluminum	10000	218	3.774×10^{7}
lead	10000	34.8	2.06×10^{10}
silicone rubber	2.8	0.27	10^{-14}

2) TYPICAL TERMINAL DEFECTS

At a location 2 cm above the base surface of the stress cone, a scratch defect measuring L × W of 2 mm × 1 mm is created on its main insulation surface. Relative permittivity, electrical conductivity, and thermal conductivity values for air gaps are set to 1, 0 S/m, and 0.023 W/(m·K^{-1}).



(a) main insulation scratch (b) semiconductive tip (c) insulation layer impurity (d) missing copper mesh

FIGURE 4. Terminal typical defect model.

3) GRID PARTITIONING

For grid division models, in regions with high field strength variations or large bend radii—such as interfaces between model layers, stress cones, and near defects—to enhance computational accuracy, as shown in FIGURE 5.

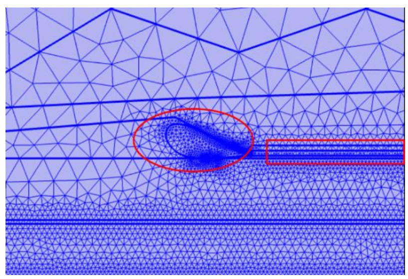


FIGURE 5. Mesh generation.

III. ELECTRIC FIELD CHARACTERISTICS AT DEFECT SITES IN INSULATION

A. MAIN INSULATION SCRATCH

As shown in FIGURE 6, during normal operation, field strength gradually decreases from the interior toward the exterior of the cable terminations. Due to differences in dielectric constants, an abnormal distribution occurs in electric fields at the interface where the main insulation meets the stress cone, resulting in a peak field strength of 5.47×10^6 V/m at the base of the stress cone.

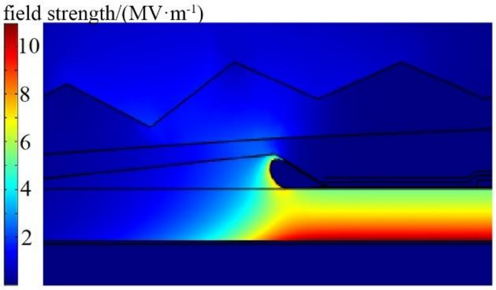


FIGURE 6. Electric field distribution cloud map in normal operating conditions.

FIGURE 7 shows that scratches on main insulation cause field distortion within the air gap, while the surrounding area remains largely unaffected. FIGURE 8 further reveals that peak field strength at defective points surges from 5.64×10^6 V/m to 1.45×10^7 V/m, exceeding air's breakdown strength (3×10^6 V/m). This makes the interior of the air gap highly susceptible to partial discharge. In the initial stage, the discharge has a minor impact on the main insulation. However, during sustained discharge, the insulating layer surrounding the air gap also begins to show signs of discharge, which accelerates the degradation of the cable insulation and reduces the insulation strength at the terminal.

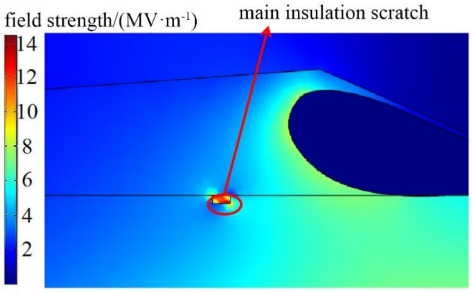


FIGURE 7. Electric field distribution cloud map of main insulator scratches.

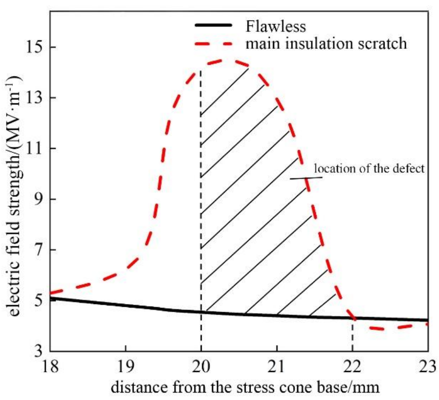


FIGURE 8. Electric field distribution curve of main insulation scratches.

B. SEMICONDUCTIVE TIP

For a terminal containing a semiconductor tip defect, its field distribution is shown in FIGURE 9. The presence of the tip causes discontinuity in the dielectric material at that location, leading to an increase in field strength. The field strength at the tip (2.21×10^7 V/m) reaches 6.72 times that under defect-free conditions (2.86×10^6 V/m), indicating severe field distortion.

As shown in FIGURE 10, the field strength at the tip exhibits more severe distortion compared to when the main insulation is scratched. On one hand, the tip's location itself is prone to charge accumulation. On the other hand, the absence of the semiconductive layer at the tip prevents uniform electric field distribution, leading to greater field concentration within the tip. The presence of the tip readily triggers partial discharge. Prolonged discharge can form minute discharge channels near the tip. When a discharge channel entirely penetrates the insulation layer, it will lead to insulation breakdown.

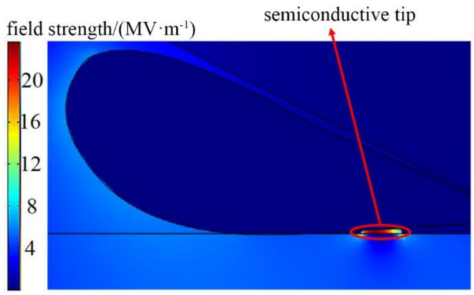


FIGURE 9. Electric field distribution cloud map of semiconductor tips.

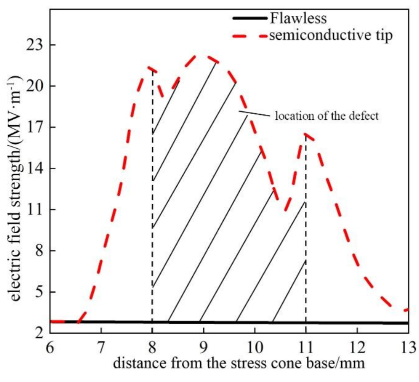


FIGURE 10. Electric field distribution curve of semiconductor tips.

C. INSULATION LAYER IMPURITY

When an insulation layer impurity is present, the electric field distribution is shown in FIGURE 11. A floating potential forms around the impurity, leading to electric field concentration. The field strength increases from 4.43×10^6 V/m to 10.02×10^6 V/m, resulting in field distortion. As shown in FIGURE 12, compared with the main insulation scratch, the impurity in the insulation layer has a higher permittivity than the stress cone cover. This causes the field strength inside the impurity to decrease, while the field distortion induced by the impurity is concentrated in the surrounding insulation material.

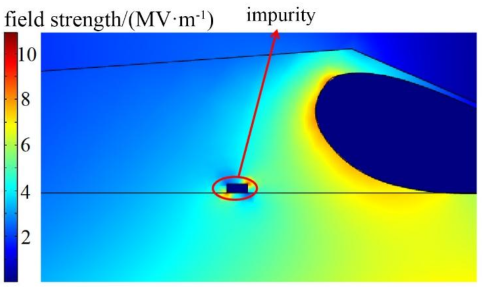


FIGURE 11. Electric field distribution cloud map of insulation layer impurity.

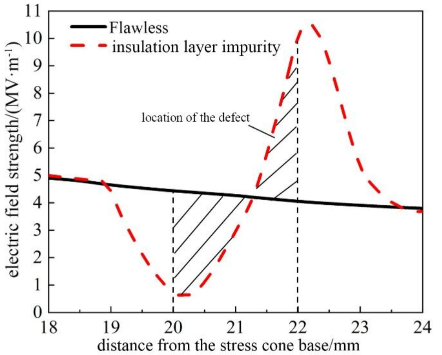


FIGURE 12. Electric field distribution curve of insulation layer impurity.

Practical engineering defects vary in severity, necessitating an investigation into their dimensional impact. Dimensions were set at 2–6 mm with 0.5 mm increments, yielding the results shown in FIGURE 13.

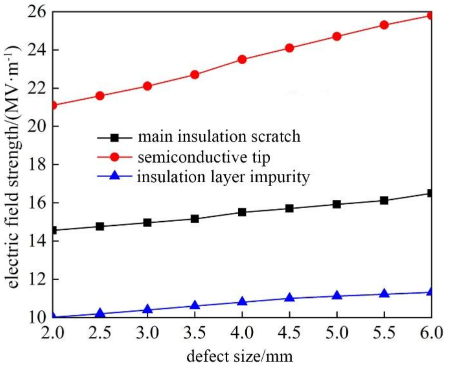


FIGURE 13. Relationship between defect size and field strength.

When defect dimensions range within 2–6 mm, maximum field strengths at the aforementioned three types of defects gradually rises, with the semiconductive tip causing the most significant change in field strength. When the field distortion exceeds the breakdown strength of the insulation medium, it will lead to insulation breakdown. After partial insulation breakdown occurs, the surrounding intact insulation will be subjected to a higher electric field, further triggering partial discharge. This ultimately forms a discharge channel and results in terminal breakdown. Therefore, during cable terminal manufacturing, care must be taken to avoid large-area defects, and particular attention should be paid to checking for the presence of semiconductive tips.

The defect location was set to 20 mm–50 mm from the bottom of the stress cone, with a step size of 5 mm, to analyze its influence. The results are shown in FIGURE 14.

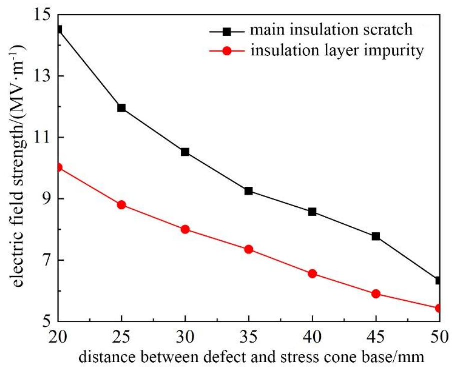


FIGURE 14. Relationship between defect location and field strength.

When the axial distance of the defect increases from 20 mm to 50 mm, reduced from 1.45×10^7 V/m and 10.02×10^6 V/m to 6.33×10^6 V/m and 5.43×10^6 V/m respectively at the main insulation scratch and impurity site within the insulation layer. This decrease resulted from moving away from the high-field region near the base of the stress cone. Therefore, during actual terminal manufacturing, special attention should be paid to whether any defects exist near the stress cone base.

IV. TEMPERATURE DISTRIBUTION CHARACTERISTICS OF INSULATION DEFECTS

FIGURE 15 illustrates the temperature gradient during normal operation: temperatures decrease sequentially from the copper core (69.3°C) to the insulating oil (31.8°C) and finally to the ambient environment (20°C). Metal at the top of the terminal heats up faster, so its temperature is lower than at the bottom.

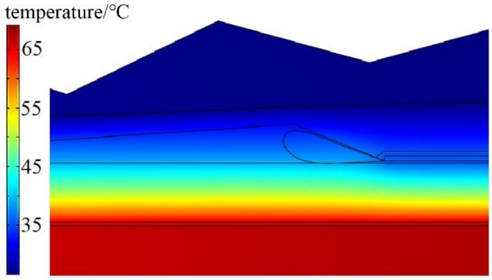
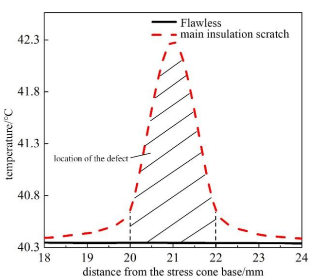
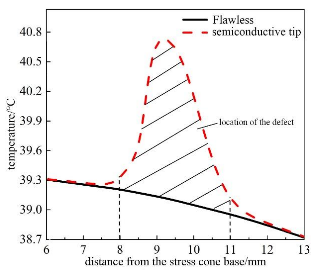


FIGURE 15. Insulation defect temperature distribution curve.

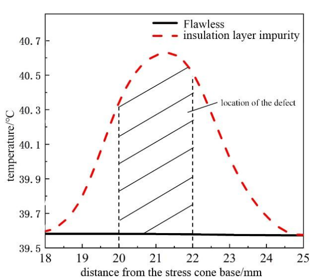
FIGURE 16 depicts the temperature distribution at the insulation defect. All three types of defects can cause an isolated layer to experience a minor temperature increase. For the main insulation scratch and the semiconductive tip defects, the insulation layer temperature rises by 1.94°C and 1.61°C, respectively. The temperature rise caused by the impurity is relatively smaller, at 1°C. The greater the difference in thermal conductivity between the defective material and the surrounding insulation, the higher the resulting temperature rise. Among the three types of defects, the difference in thermal conductivity from highest to lowest is: scratches on the main insulation, tips of the semiconductive layer, and impurities. Therefore, the temperature rise decreases in that order. As the temperature at the defect site increases, insulation layer properties gradually deteriorate, leading to redistribution of fields and the occurrence of partial discharge phenomena. The heat generated by sustained partial discharge causes the temperature to rise further, accelerating insulation deterioration and ultimately leading to insulation failure.



(a) main insulation scratch



(b) semiconductive tip



(c) insulation layer impurity

FIGURE 16. Insulation defect temperature distribution curve.

FIGURE 17 shows a stepwise increase in temperature for all three defect types when the defect size range is 2–6 mm. When the defect size is smaller than 4 mm, the temperature rise caused by the main insulation scratch is greater than that caused by the semiconductive tip and the insulation layer impurity. When the defect size exceeds 4 mm, the temperature rise induced by the semiconductive tip becomes greater than that of the other two defects. This is because the semiconductive tip causes more severe electric field distortion than the other two defect types, resulting in relatively greater heat generation.

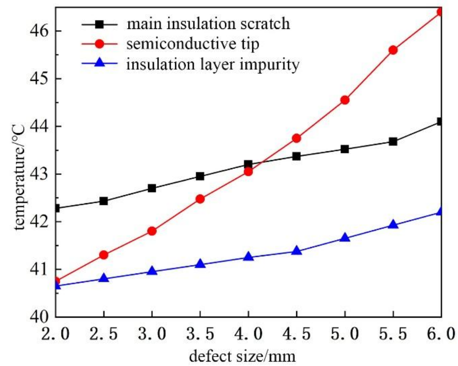


FIGURE 17. Relationship between defect size and temperature.

The ambient temperature is set at 20–40°C with a step size of 5°C to investigate how temperature affects the insulation layer at defect locations. The results are shown in FIGURE 18. Higher temperatures resulted in higher insulation layer temperatures at defect locations: below 25°C, all three defects exhibited similar temperature rise magnitudes; above 25°C, both main insulation scratches and semiconducting tips caused greater temperature rises than insulation layer impurities, with main insulation scratches showing the most significant temperature increase.

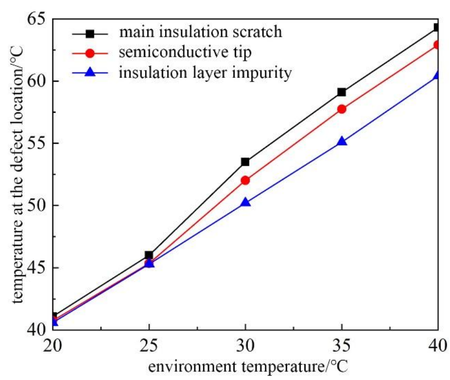
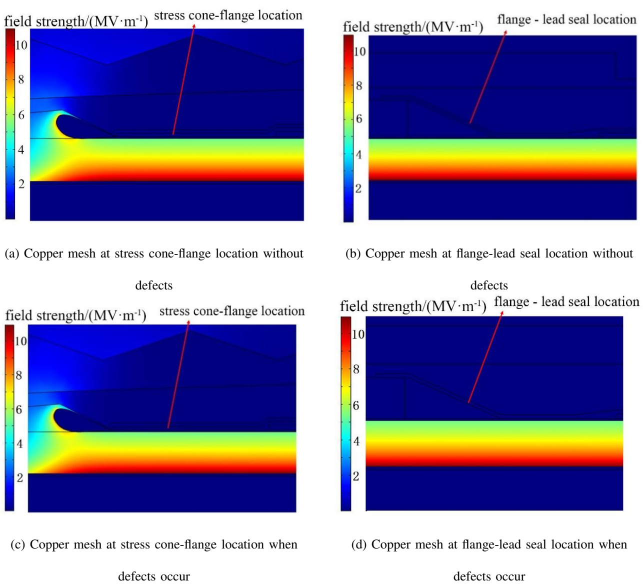


FIGURE 18. Effect of external temperature on insulation layer temperature under defects.

V. MISSING COPPER MESH

A. MISSING COPPER MESH ELECTROFIELD SIMULATION

When the terminal lacks a copper mesh, as shown in FIGURE 19, it exhibits the following electrical field distributions. When there is no copper mesh, the field strength at that spot goes up a little. FIGURE 20 shows this. Maximum field strength reaches 1.6 kV/m without copper mesh at stress cone flange locations. For a missing copper mesh at the flange-lead seal location, the highest field strength is 0.24 kV/m. When the copper mesh is missing, the outer semiconductive layer at that location remains ungrounded, creating a floating potential that distorts the electric field. Since the semiconductor layer at the missing copper mesh still connects to the copper sleeve and the semiconductor itself acts to equalize electric fields, the field distortion caused by this grounding system defect is relatively small compared to that caused by insulation-type defects. However, under long-term exposure to the distorted electric field, air discharge may occur inside the tail. The damage resulting from such discharge can make the outer semiconductive layer uneven, further exacerbating the electric field distortion.



(a) Copper mesh at stress cone-flange location without defects

(b) Copper mesh at flange-lead seal location without defects

(c) Copper mesh at stress cone-flange location when defects occur

(d) Copper mesh at flange-lead seal location when defects occur

FIGURE 19. Electric field distribution cloud map of missing copper mesh.

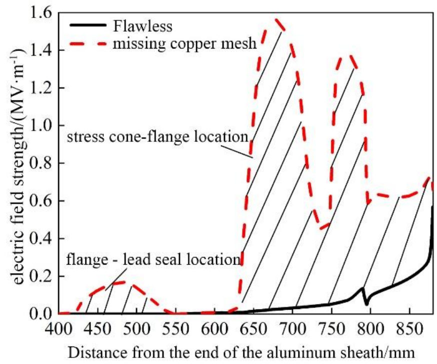
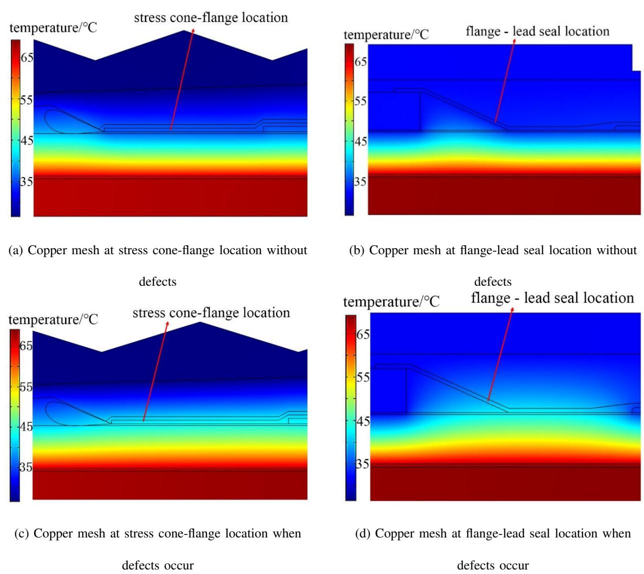


FIGURE 20. Electric field distribution curve of missing copper mesh.

B. MISSING COPPER MESH TEMPERATURE SIMULATION

As shown in FIGURE 21, the temperature at the copper mesh defect location is higher than normal conditions. FIGURE 22 indicates that due to the high thermal conductivity of the copper mesh, temperatures rise by 7.4°C and 8.7°C respectively at the stress cone-flange and flange-lead seal locations lacking copper mesh. After the copper mesh is missing, the material at that location becomes air, which has a much lower thermal conductivity. Therefore, compared to insulation-type defects, grounding system defects result in a higher temperature rise. The temperature increase will degrade the performance of the insulation layer, thereby accelerating the process of electric field distortion, triggering partial discharge, and further leading to insulation damage. Hence, during actual terminal manufacturing, care should be taken to avoid the occurrence of grounding system defects.



(a) Copper mesh at stress cone-flange location without defects

(b) Copper mesh at flange-lead seal location without defects

(c) Copper mesh at stress cone-flange location when defects occur

(d) Copper mesh at flange-lead seal location when defects occur

FIGURE 21. Temperature distribution cloud map of missing copper mesh.

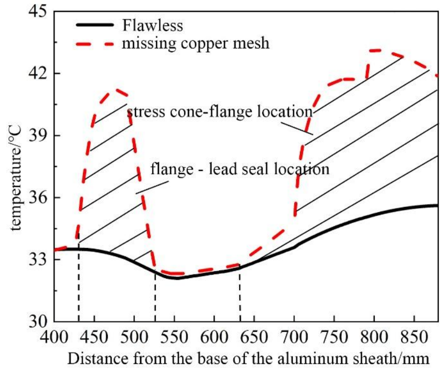


FIGURE 22. Temperature distribution curve of missing copper mesh.

VI. CONCLUSION

This paper conducts a simulation analysis of the electrothermal coupling field in four typical defects within cable terminations, researching how different defects influate the terminal electric field and temperature patterns. The conclusions are as follows:

(1) Insulation defects make the electric field increase. The field distortion from the semiconductive tip is the most serious. It makes the electric field strength go up by 6.72 times. The main insulation scratch and the insulation layer impurity increase field strength by 1.57 times and 1.26 times, respectively, at the defect locations. The electric field gets bigger when the defect size is bigger. Also, the electric field is stronger when the defect is closer to the bottom part of the stress cone.

(2) The presence of insulation defects causes a slight temperature rise. The main insulation scratch and the semiconductive tip raise the temperature at the defect by 1.94°C and 1.61°C, respectively, while the insulation layer impurity raises it by 1°C. With increasing defect size, local temperatures gradually rise. When defect size exceeds 4 mm, the temperature rise induced by the semiconductive tip becomes greater than that caused by the other two defects. Simultaneously, the temperature at the defect location increases with rising ambient temperature.

(3) Compared to insulation defects, the electric field distortion caused by a missing copper mesh is relatively small, but the resulting temperature rise is comparatively larger, with a maximum value of 8.7°C. Prolonged operation under such conditions can easily lead to insulation failure, resulting in terminal breakdown.

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