

Development of X-Band Transceiver MMIC's Using GaN Technology

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Abstract

This paper describes X-Band power amplifier (PA), low noise amplifier (LNA) and switches that can be used in transmit/receive modules which are developed with GaN technology. For Transmit chain two 25 W high power amplifiers that are tuned between 8-10 GHz and 10-12 GHz bands are designed. A low noise amplifier with 2 W survivability and less than 2dB noise figure is designed for receive chain. Furthermore, an RF switch that is capable of withstanding 25 W RF power is developed for the selection of transmit or receive chains. Measurement results show that both power amplifiers produce 25 W of power. Low noise amplifier has more than 20 dB small signal gain with less than 2 dB noise figure. RF switch has 50 dB of isolation with less than 1 dB insertion loss.

1. Introduction

High power capability is an important aspect of nowadays transceiver IC designs. Traditionally, these integrated circuits are developed using CMOS and GaAs processes. However, these technologies have a low power handling capability which is mostly limited at 1 W. Newly emerging III-V semiconductor technologies which includes GaN material can produce large powers in a small area compared to traditional CMOS and GaAs, [1]. Due to its high bandgap energy, which is approximately three times more than Si and GaAs, can obtain higher breakdown voltages as well as high drain voltages. This high drain voltage forming a power density of 5 W/mm from a single transistor creates a great design advantage when compared to other technologies [2]. In addition to this, passive circuits that utilize these transistors can withstand higher power and voltage swings than other semiconductor materials [3], [4].

When electronic warfare is considered, which is a typical application of X-band transceiver circuits, circuits must be able to produce high power in a limited area and they must be protected from high power RF signals exposed from other systems. Conventional transceiver architecture is given in Fig. 1(a). For protecting circuits from high power RF exposure, receiver circuits typically contain a limiter before the receiver LNA as shown in the figure. These limiters are generally produced at a different semiconductor technology which makes them hard to integrate on a same substrate with other components. Moreover, they limit the performance of the receiver by reducing the bandwidth and increasing noise

figure as they are placed before the receiver LNA. By utilizing GaN transistors in the LNA, these limiters can become obsolete as the GaN transistors can now withstand high input powers without a need of an external limiter. By offering comparable gain and noise figure with other semiconductor technologies GaN makes an excellent replacement for a receiver design [5-8].

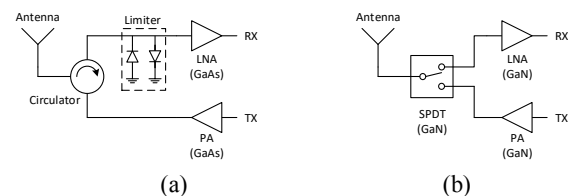


Figure 1: A general transceiver architecture (a) conventional (b) with GaN technology

High power handling can also be used at the design of RF switches. As these switches are connected at the output of the power amplifier, they can be able to withstand high power signals. GaN transistors can increase this power handling limit thus enabling high power switch design in an MMIC[3]. In the end, by removing the limiter and eliminating the need of a circulator due to high power resistant switches, all T/R module including SPDT, PA and LNA can be implemented on the same die as given in Fig. 1(b). This gives an advantage of full integration of the transceiver module on the same die.

This paper presents X-band transmitter and receiver blocks which are and two power amplifiers that can produce 25 W, an LNA and a switch which are designed on GaN process. The schematic design, simulation and measurement results are given for the designed MMICs thus proving dedicated operation. These IC's are produced using "0.25 μ m Power GaN/SiC HEMT" process of WIN Semiconductors.

2. Power Amplifier Design and Results

For PA, two separate circuits are designed for X-Band coverage. First design covers a frequency range of 8–10 GHz and second design covers a range of 10–12 GHz. With these two circuits all of the X-band is covered and both designs can produce 25 W of RF power.

2.1. Power Amplifier Design

For this particular case, a class AB amplifier biasing is chosen. As the output power is high, low efficiencies would

generate a high power dissipation on the MMIC thus a powerful cooling would be required. However, class B biasing would cause the transistor to operate at a higher nonlinear distortion which is not desired. Therefore, class AB biasing is a good compromise between the linearity and efficiency of the amplifier.

Since 25 W output power is desired, 8 transistors are used at the output for both of the designs. As each transistor can provide a power at the output around 5 W, 8 transistors ideally would provide 40 W. However, when the combining losses are considered these 8 transistors are enough to provide a power around 25 W.

In order to determine the output impedance for maximum power output, a series load pull simulation is performed on the transistors. In these simulations, the transistor sizes, bias currents are optimized to achieve a reasonable power output with power added efficiency (PAE). A load pull simulation results are given in the Fig. 2. In this simulation two transistors which are sized as 6x125 μm and 8x125 μm are used. For 6x125 μm , the load impedance is calculated as $13.4+25.8j \Omega$ which is used in the design of 8-10 GHz amplifier. For 8x125 μm , the load impedance is calculated as $7.8+20.2j \Omega$ which is used in the design of 8-10 GHz amplifier.

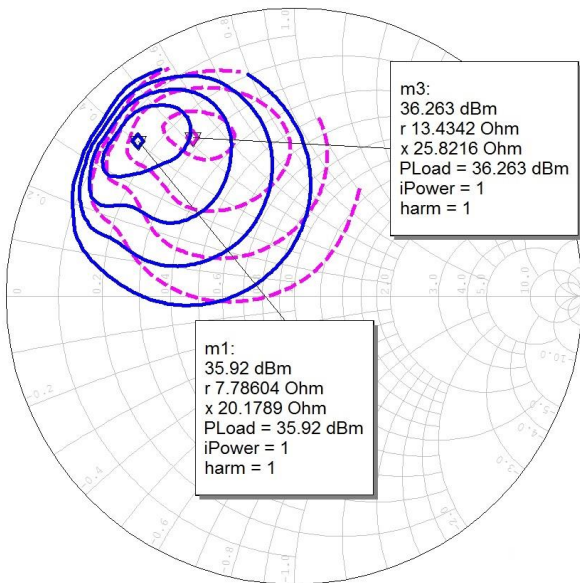


Figure 2: Load pull simulation results for two transistors size 6x125 μm (purple dashed line) and 8x125 μm (blue solid line)

Matching circuit design consists of many L-C low pass matching sections. Due to practical high sizes of inductors and low Q factors inside an MMIC, these inductors are implemented as transmission lines. A simplified schematic for the 8-10 GHz design is given in Fig. 3.

DC biases are implemented in two fashions. For gate biases, a resistance between 40-100 Ω is added in series to the gate and a choke inductor greater than 3 nH is added after this transistor in series. A sample schematic is given in Fig. 4. For drain biases, these paths must carry large amount of

currents which are not suitable for these inductors due to thin metal lines. Therefore they are implemented using a quarterwave length transmission lines. Moreover no resistance is used at drain biases as due to large current withdrawal, they would both cause a voltage drop at the output and they would eventually result in a power loss which is highly undesirable. Both of these lines are terminated with high decoupling capacitors close to the DC power pads.

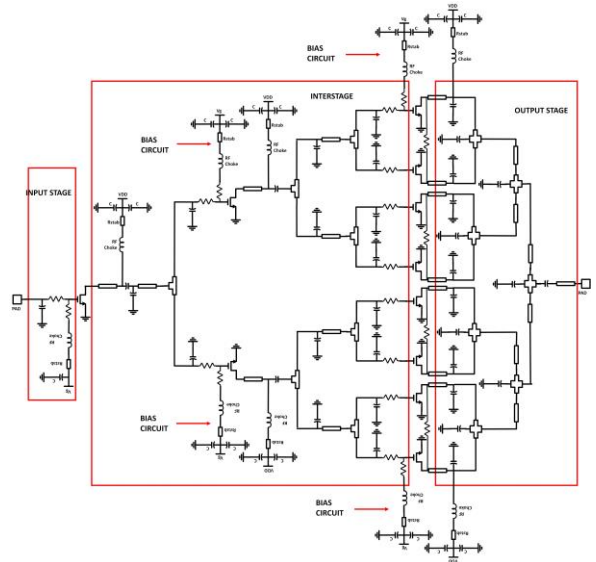


Figure 3: Schematic for 3 stage 8-10 GHz PA design

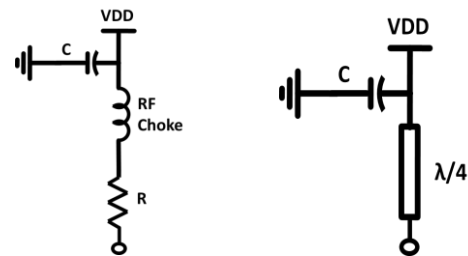


Figure 4: Schematic of gate DC bias line (left side) and drain DC bias line (right side)

Stability is an important concept for a power amplifier. As precautions for stability, a series of circuit techniques are applied. First of all, a series small resistance in the order of 2-4 Ω are added before each transistor gate. This resistance would decrease the effect of any positive feedback by reducing the transistor gain. Secondly bias resistance at the gate DC bias lines helps achieving the stability by maintaining a constant impedance at the input transistor hence becoming more tolerant to changes in input impedances. Lastly, an even-odd mode resistor in the order of 100 Ω is added at the output stage to maintain a balance between transistors even if there is a process variation between these transistors. A sample schematic showing all these stability methods are given in Fig. 5. In the Fig. 5, R1 shows the series resistance at the bias line, R2 represents the

series resistance at the gate of the transistors and R3 denotes an even-odd mode resistance.

All of the matching circuits along with their DC bias lines are simulated using AXIEM, a 2D method of moments electromagnetic solver. In addition to this, the PCB interconnects up to SMA's are simulated using ANALYST, a 3D finite element method electromagnetic solver. Fig. 6 shows 3D simulation of interconnects between MMIC and PCB.

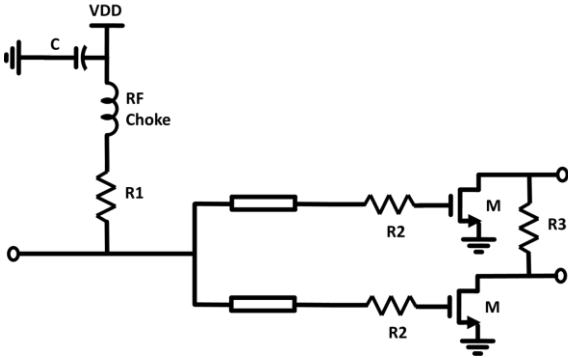


Figure 5: Schematic for stability resistances

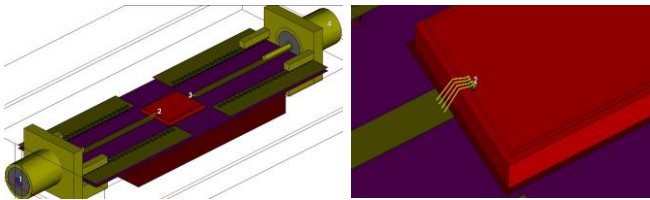


Figure 6: 3D EM simulation setup for the PCB. Left picture full view, right picture zoomed on interconnect.

2.2. Thermal Management

With 25 W output power and a class AB biasing scheme, the efficiency of the PA is around 25%. This low efficiency causes 75% of the input DC power to be dissipated on the transistors thus increasing their temperature. This excess heat must be removed from the IC before junction temperature rises to critical values which is defined as 225 °C for this technology.

This process offers some advantages in terms of thermal management when compared to Si and GaAs. First of all, backvias are used which are direct connections from the source of the transistor to the backside metal. By this way, the heat at the junction is effectively removed. Secondly, SiC is a good heat conductor with heat conductivity of $3.5 \text{ Wcm}^{-1}\text{K}^{-1}$ [9] rather than Si and GaAs which also improves efficiency of the overall heat removal process. However, due to high power levels, a cooler is designed since these structures are not still enough to dissipate all the power.

An assembly is designed with a cooler to remove the heat effectively. The assembly consists of a copper plate to effectively dissipate heat and an active cooler with a fan. PA MMIC is attached to this assembly using AuSn epoxy with high thermal conductivity around $60 \text{ Wcm}^{-1}\text{K}^{-1}$. [10] The picture of the assembly is given in Fig. 7.

Fig. 8 shows the thermal analysis of the structure at 25 °C ambient. From top to bottom, the material stackup is defined as 100 μm SiC, 10 μm AuSn epoxy, copper surface and active cooling convection parameter at the bottom side of the copper. At 25 °C ambient, the maximum temperature is given as 93 °C.

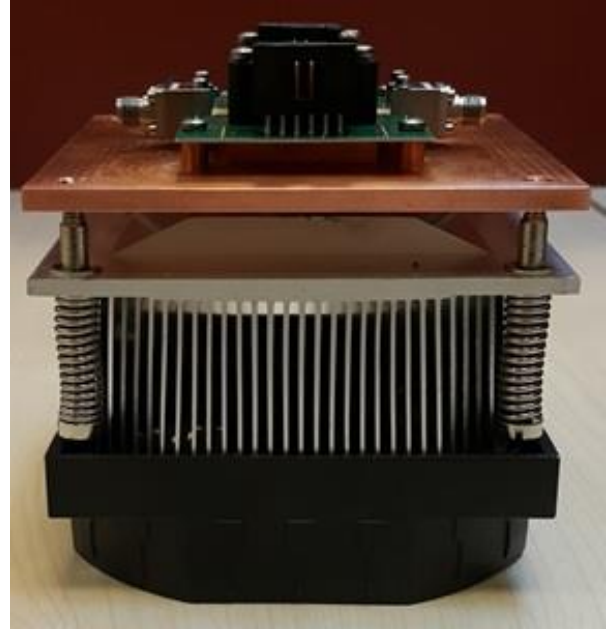


Figure 7: Assembly of cooler

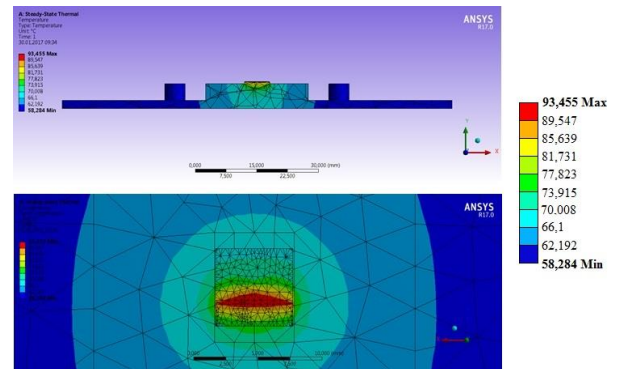


Figure 8: Thermal simulation results at 25 °C ambient. Top picture front view and bottom picture top view. Maximum temperature is 93 °C.

2.3. Manufactured Assembly and Measurement Results

Designed PA's are produced using "0.25 μm Power GaN/SiC HEMT" process of WIN Semiconductors. Manufactured and assembled die photos are given in Fig. 9 and Fig. 10. Both die sizes are equal which are 6.3 mm by 5.0 mm.

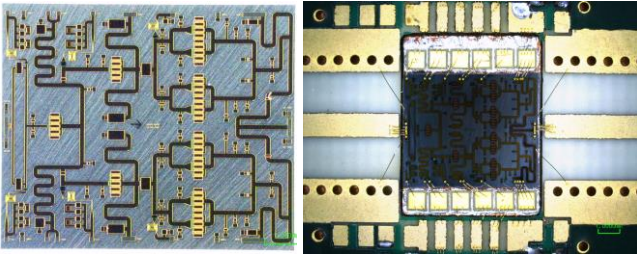


Figure 9: Manufactured PA MMIC at 8-10 GHz and placement on the PCB

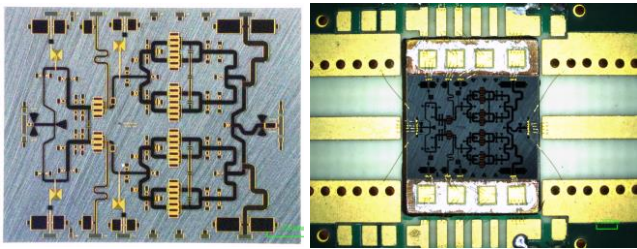


Figure 10: Manufactured PA MMIC at 10-12 GHz and placement on the PCB

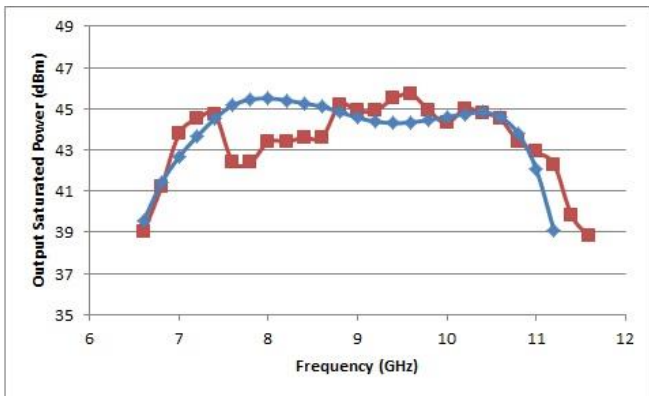


Figure 11: Saturated power output for amplifier operating between 8-10 GHz. Blue line: simulation, red line: measurement

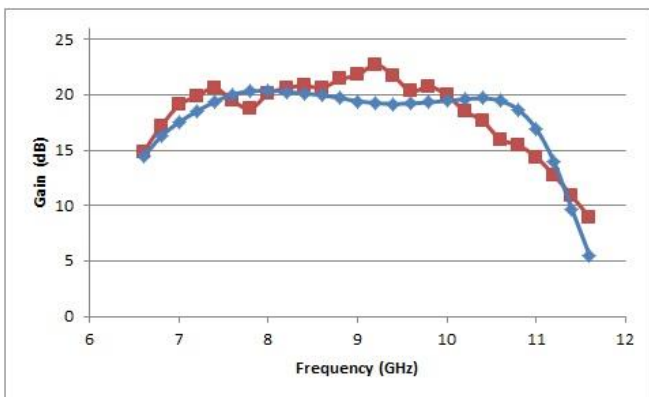


Figure 12: Power gain for amplifier operating between 8-10 GHz. Blue line: simulation, red line: measurement

The measurement results along with the simulation results are provided in Fig. 11 to Fig. 16. All of the simulations and measurements are done in continuous wave. From the figures it can be deduced that both chips provide an output power greater than 25 W with more than 25% power added efficiency. Measurement results are in accordance with the simulation results with only minor differences in the characteristics.

2.4. Comparison with other state of the art

Table 1 gives a comparison between the state of the art X-band PA's in literature. When compared with them, our design achieves a good tradeoff between bandwidth and power and efficiency while providing power outputs up to 30 W.

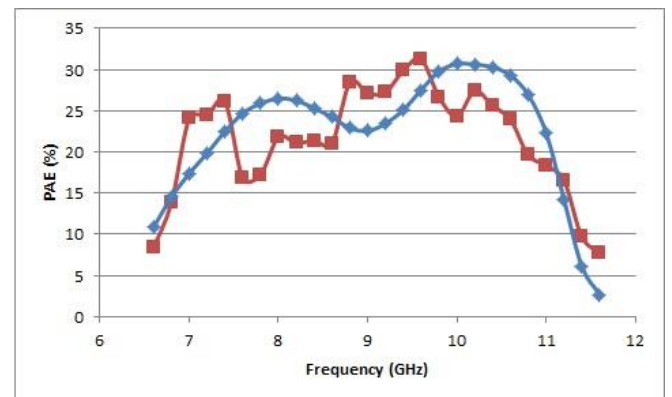


Figure 13: Power added efficiency for amplifier operating between 8-10 GHz. Blue line: simulation, red line: measurement

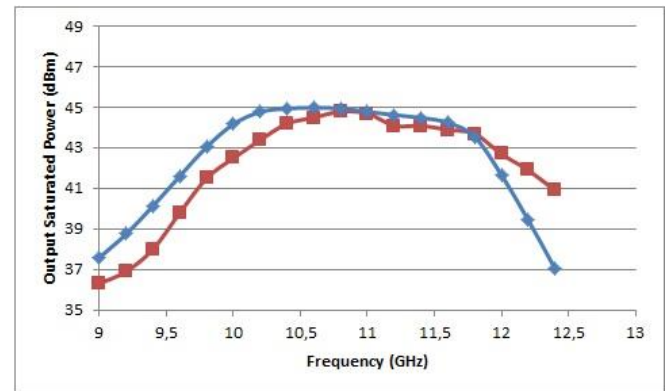


Figure 14: Saturated power output for amplifier operating between 10-12 GHz. Blue line: simulation, red line: measurement

3. Low Noise Amplifier Design and Results

The design specifications for the LNA can be listed as follows. The gain of the amplifier must be higher than 20 dB and noise figure must be lower than 2 dB to be comparable with its CMOS and GaAs counterparts. Moreover, it must be able to withstand 2 W of RF input power.

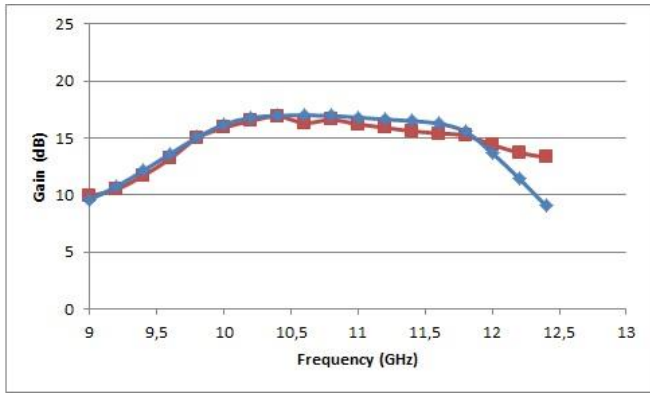


Figure 15: Power gain for amplifier operating between 10-12 GHz. Blue line: simulation, red line: measurement

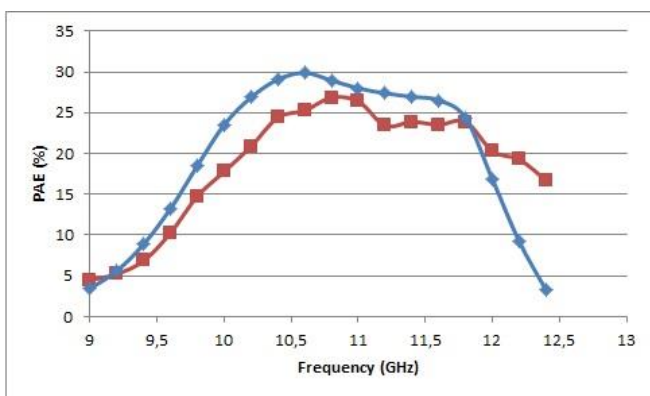


Figure 16: Power added efficiency for amplifier operating between 10-12 GHz. Blue line: simulation, red line: measurement

Table 1: Comparison with other state of the art

Rf.	Package	Meas. Type	Vds (V)	Freq. (GHz)	Pout (W)	PAE (%)	Gain (dB)
[11]	Packaged	Pulsed	50	9.5-10.0	25.0	40	12.0
[12]	Packaged	CW	40	9.5-10.5	5.4	38	15.0
[13]	Packaged	CW	25	10.0-10.5	14.0	61	19.0
[14]	N/A	Pulsed	35	6.0-18.0	20.0	15	9.6
[15]	On-Wafer	Pulsed	36	7.0-11.0	40.0	38	16.5
8-10 GHz	Packaged	CW	28	7.0-11.0	30.0	30	21.0
10-12 GHz	Packaged	CW	28	10.0-12.0	25.0	27	17.0

3.1. LNA Design

LNA is designed as a 3 stage to meet the gain requirements of the amplifier. The second critical parameter is that the amplifier can be able to withstand an RF power more than 2 W. By using the technology set limits for maximum voltage and current ratings, the required size of the input transistor is

calculated as 200 μm and this transistor is used in the design. Moreover using this small sized transistor allows the designer to implement a low noise design. As the input transistor is the highest contributor to the noise figure of the LNA, the transistor that can provide the least amount of noise is preferred.

Schematic design, shown in Fig.17, follows a cascaded 3 stages common source amplifier inductive degeneration. Inductive degeneration is selected to both achieve a low noise figure and a good input matching in this design. For this design a core single stage amplifier is designed and these core amplifiers are cascaded 3 times.

To improve the stability of the amplifier, additional shunt resistive feedback is used at each stage which is also shown in the Fig. 17.

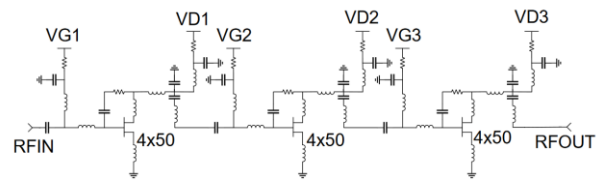


Figure 17: Schematic of LNA Design

The whole amplifier is simulated using AXIEM. As the inductors used in the design can be coupled to each other due to tight placement, their effects must be simulated. Furthermore, using these results in EM analysis, the layout is optimized for best performance and smallest size. Manufactured die photograph is given in Fig. 18.

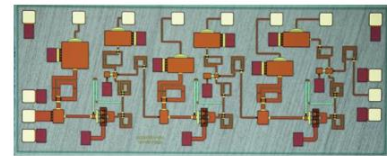


Figure 18: Manufactured LNA die photo. Size is 2.8 x 1.3 mm²

3.2. LNA Measurement Results

Manufactured dies are measured using on wafer measurement techniques. Measurement results with comparison to simulation results are provided in Fig. 19 and Fig. 20. From S parameter results, it can be seen that the amplifier has more than 20 dB gain and all the reflection parameters are under 5 dB. Moreover the noise figure is below 2 dB which is comparable to many commercial amplifiers covering whole X-band.

Power handling capacity is measured by providing 2 W of input power to the LNA and measuring the change in NF and gain after power is applied. During the test conditions the change in the noise figure and gain is limited to less than 0.5 dB which shows a robust LNA that can withstand at least 2 W of input power.

This GaN process is still under development by the foundry, which is the main reason for the small discrepancies between the simulation and the measurement

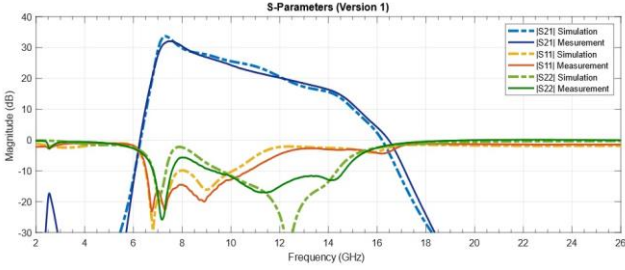


Figure 19: S parameter results of the LNA. Dashed line simulation and solid line measurement

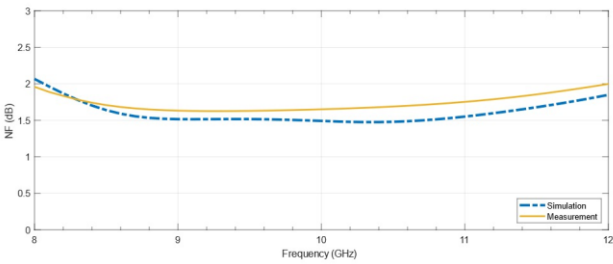


Figure 20: Noise figure results of the LNA. Dashed line simulation and solid line measurement

results. This small discrepancy is due to the transistor models only, as the measurement of passive structures matches very well with the simulated values. The three-stage topology achieves high linearity, providing an OIP3 of 29 dBm at 0.6 W power dissipation.

3.3. Comparison of LNA with state of the art

Performance of the LNA is compared with performance of LNAs available in literature in Table 2. It is observed that the performance of the circuit is comparable to the other LNAs recently reported in the literature in terms of bandwidth, noise and gain.

Table 2: Comparison of LNA with state of the art

Ref.	Freq. (GHz)	NF (dB)	Gain (dB)	S11 (dB)	Pdc (mW)
[16]	4-16	1.45	11	10	-
[17]	7-12	2.5	14	10	-
[18]	8-12	1.8	14	-	210
[18]	7-11	2.0	18	-	350
[19]	8-10	1.3	24	2	900
[19]	10-12	1.3	24.4	10	900
This work	8-11	1.6	22	9.1	600

4. High Power Switch Design

In order to use a switch with the designed power amplifier, an SPDT switch that can withstand 25 W is designed. For power handling purposes a few changes are made rather than traditional series shunt switch design.

4.1. High Power RF SPDT Switch Design

Schematic of the designed switch is provided in Fig. 21. The switch consists of quarterwave transmission lines, shunt inductors and shunt transistors only. Series switches have a power handling penalty than the shunt switches because all of the transmitted power goes through the drain and source terminals of the transistors hence dissipating power on the transistor. The aim of using shunt transistors with quarterwave transistors is to provide low voltage swing across switch terminals and therefore increasing its power handling capability.

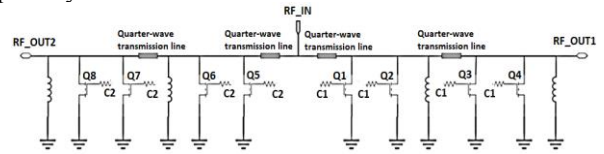


Figure 21: Schematic of the switch design

For ON path, where the transistors are turned OFF, the signal would follow the transmission line to the output. The OFF capacitance of the transistors are resonated with an inductor to ensure minimum power is transmitted on the switches, both lowering insertion loss and increasing power handling. When the OFF path is considered, the transistors are turned ON and connected to ground. Quarterwave transmission line can convert this low impedance into a high impedance at the common port therefore reducing signal leakage on the OFF path.

The GaN transistors used in this design are depletion type transistors and they have a threshold voltage around -3 V. At 0 V, the transistors are turned on and at -40 V they are turned off. This high turn off voltage allows a high linearity in the transistor as any voltage swing across drain or source terminal will be coupled to gate ensuring the transistor is turned OFF even at the highest voltage swings. Moreover, due to their high breakdown voltage around 100 V, these transistors would withstand any voltage swing that is less than 100 V.

All the transistor sizes, inductor placement and quarterwave transmission lines are optimized using a 2D electromagnetic solver provided by ADS. To satisfy the power requirements, harmonic balance simulations are used. After obtaining current and voltage waveforms, breakdown limits set by the foundry are checked and design is modified accordingly to work under 25 W of RF input.

4.2. Manufactured Switch and Results

Die photograph of the switch, which was fabricated by WIN Semiconductors, is presented in Fig. 22. Overall size of the switch is 4.1×2.7 mm².

4 samples of switch are measured for characterization using on wafer measurements. Small signal parameters that are measured are given in Fig. 23 to Fig. 25. The insertion loss is around 0.8 dB at the whole X-Band and reflection parameters are all below -10 dB. The isolation of the OFF path is greater than 50 dB at the band of interest.

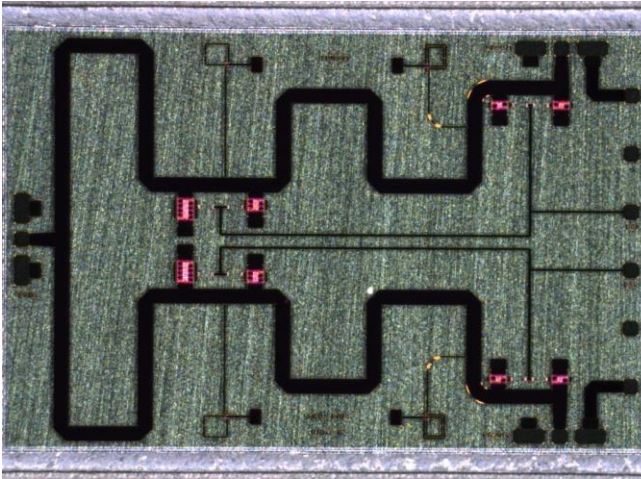


Figure 22: Die photo of the switch

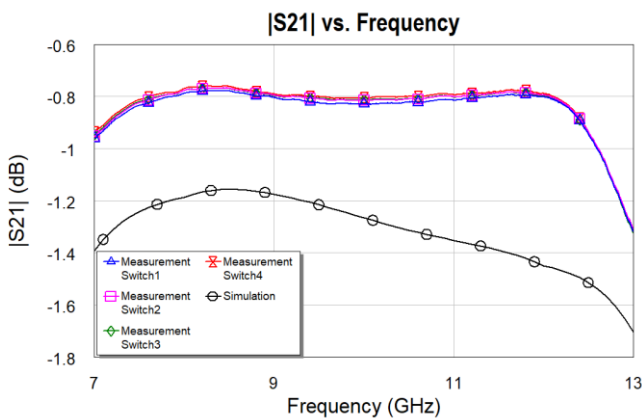


Figure 23: Insertion Loss for the designed switch. Black line simulation. Other lines measurement

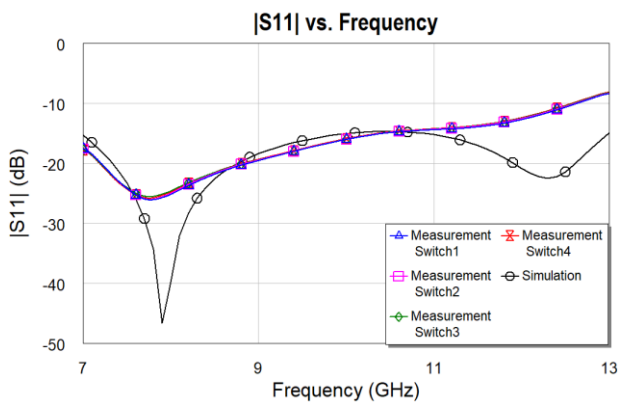


Figure 24: Reflection for the designed switch. Black line simulation. Other lines measurement

To characterize the power handling capacity of the switch, a PCB is designed and manufactured. The fabricated PCB is a single layer PCB using a 20 mil thick RO4003C material. A power amplifier is connected to the common port of this switch and 25 W of continuous wave is pushed to the switch. The maximum output power of the amplifier is

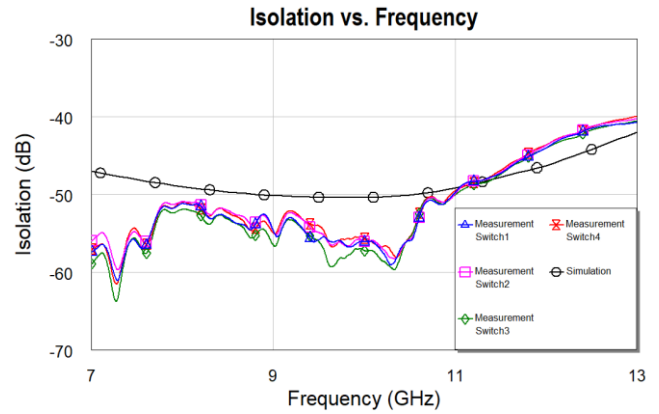


Figure 25: Isolation for the designed switch. Black line simulation. Other lines measurement.

43.6 dBm and that was the limit of this test setup. Under this power rating, the switch doesn't have any change in s-parameters, hence it can withstand 43.6 dBm power. Moreover, measured P_{1dB} at 10.6 GHz is at 43.3 dBm.

This switch transistor process and modeling is under development by the foundry during the time of manufacturing. Therefore there are some mismatches between simulation and measurement results but yet they are welcome in this occasion. To verify the measurements, the samples are measured at different institutions yet the results are the same.

4.1. Comparison of Switch with Other State of the Art

Table 3: Comparison of switch with other state of the art

Ref.	Freq. (GHz)	IL (dB)	Iso. (dB)	RL (dB)	P_{1dB} (dBm)
[3]	0-12	1.0	30	12	-
[3]	0-18	1.5	25	12	-
[20]	8-11	3.5	30	10	44.0
[21]	0-12	1.2	30	-	39.2
[22]	8-12	2.0	35	15	37.0
[23]	0-12	1.4	20	15	-
[24]	8-11	1.0	37	13	39.5
[25]	2-18	2.2	25	11	38.5
[26]	6-18	1.0	35	10	45.0
This Work	8-12	0.8	44	13	43.3

Some published results for X-band switches up to 18 GHz are presented in Table 3 and compared with this work. From the results our switch has a high isolation and linearity when compared to the other works. In addition to its superior isolation and linearity, it has very low insertion loss when compared to other switches in interest.

5. Conclusion and Future Work

Throughout this work, various MMICs in X-band are designed using a commercial 0.25 μm GaN on SiC process. A high power resistant LNA, a high power handling switch and two high power amplifiers are designed and measured.

Measurement results verify the operation of all of the designed MMIC's.

The power amplifier MMIC's are developed at two different frequency bands, namely 8-10 GHz and 10-12 GHz. Both of the MMIC's achieve a power output greater than 25 W with more than 25 % PAE.

LNA MMIC design covers the whole X-Band. By handling 2 W of input power, a limiter in a conventional T/R modul designs is not required to protect the receiver if the presented GaN LNA is used. Low noise figure which is less than 2 dB, whole X-Band coverage and gain more than 20 dB shows that the presented GaN LNA has comparable performance metrics with other state of the art.

Switch MMIC can handle 25 W's of power which enables it to be used with the designed PA MMIC in a system/R module. Moreover, its low insertion loss and high isolation make it very suitable to be used in a time division duplex system or radars.

With these successful development of MMIC's, the next target is to build a transceiver MMIC which is composed of these 3 MMIC blocks described in this paper. The diagram of the system is given in the Fig. 26.

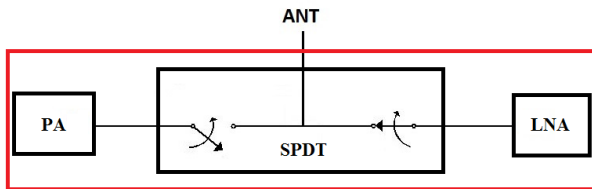


Figure 26: GaN transceiver system

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References

- [1]. C. F. Campbell, "Gallium Nitride Power MMICs Promise and Problems", Integrated Nonlinear Microwave and Millimeter-wave Circuits Workshop (INMMiC), November 2015.
- [2]. A. Katz, M. Kubak ve G. DeSalvo, "A 6 to 16 GHz Linearized GaN Power Amplifier," *2006 IEEE MTT-S International Microwave Symposium Digest*, San Francisco, California, 2006, p. 1364-1367.
- [3]. C. F. Campbell, D. C. Dumka, "Wideband high power GaN on SiC SPDT switch MMICs," *IEEE MTT-S Int. Microwave Symp. Dig.*, Anaheim, California, U.S.A, p. 145-148, May 2010.
- [4]. O. Memioglu et al., "Design and Implementation of an Encapsulated GaN X-Band Power Amplifier Family," *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Madrid, 2018, pp. 89-92.
- [5]. O. Kazan et al., "An X-Band Robust GaN Low Noise Amplifier MMIC with Sub 2 dB Noise Figure," *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Madrid, 2018, pp. 234-236.
- [6]. O. Memioglu et al., "A High Power GaN, Quarter Wave Length Switch for X-Band Applications," *2018 IEEE 18th Mediterranean Microwave Symposium (MMS)*, Istanbul, 2018, pp. 195-197.
- [7]. P. Parikh, Y. Wu, M. Moore, P. Chavarkar, Mishra, R. Neidhard, L. Kehias, T. Jenkins, "High linearity, robust, AlGaIn-GaN HEMTs for LNA and receiver ICs," *Proceedings of IEEE Lester Eastman Conference on High Performance Devices*, p. 415-421, August 2002
- [8]. U. Mishra, S. Likun, T. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, s. 287-305, February. 2008
- [9]. B. M. Green et al., "High-power broad-band AlGaIn/GaN HEMT MMICs on SiC substrates," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 12, pp. 2486-2493, Dec 2001.
- [10] Harris, J & Matthews, M. (2009). "Selecting die attach technology for high-power applications." *Power Electronics Technology*. 35. 18-23.
- [11] J. G. Leckey, "A 25W X-band GaN PA in SMT package," *2014 9th European Microwave Integrated Circuit Conference*, Rome, 2014, pp. 397-309.
- [12] S. Pavlidis, A. . Ulusoy and J. Papapolymerou, "A 5.4W X-band gallium nitride (GaN) power amplifier in an encapsulated organic package," *2015 European Microwave Conference (EuMC)*, Paris, 2015, pp. 789-792.
- [13] D. Sardin, T. Reveyrand and Z. Popovi, "X-band 10W MMIC high-gain power amplifier with up to 60% PAE," *2014 9th European Microwave Integrated Circuit Conference*, Rome, 2014, pp. 393-396.
- [14] E. Kuwata et al., "C-Ku band ultra broadband GaN MMIC amplifier with 20W output power," *Asia-Pacific Microwave Conference 2011*, Melbourne, VIC, 2011, pp. 1558-1561.
- [15] S. Piotrowicz et al., "State of the Art 58W, 38% PAE X-Band Al-GaN/GaN HEMTs Microstrip MMIC Amplifiers," *2008 IEEE Compound Semiconductor Integrated Circuits Symposium*, Monterey, CA, 2008, pp. 1-4.
- [16] M. Micovic, A. Kurdoghlian, T. Lee, R. O. Hiramoto, P. Hashimoto, A. Schmitz, I. Milosavljevic, P. J. Willadsen, W.-S. Wong, M. Antcliffe, M. Wetzel, M. Hu, M. J. Delaney, and D. H. Chow "Robust broadband (4 GHz - 16 GHz) GaN MMIC LNA," in *IEEE Compound Semiconduct. Integr. Circuits Symp.*, Oct. 14-17, 2007, pp. 1-4.
- [17] C. Andrei, R. Doerner, O. Bengtsson, S. A. Chevtchenko, W. Heinrich, and M. Rudolph, "Highly linear X-band GaN-based low-noise amplifier," in *Intl. Symp. Signals, Syst., Electron. (ISSSE)*, Oct. 3-5, 2012, pp. 1-4.
- [18] P. Schuh and R. Reber, "Robust X-band low noise limiting amplifiers," in *IEEE MTT-S Intl. Microwave Symp. Dig.*, Jun. 2-7, 2013, pp. 1-4.
- [19] M. Vittori, S. Colangeli, W. Ciccognani, A. Salvucci, G. Polli, and E. Limiti, "High performance X-band LNAs using a 0.25 um GaN technology," in *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Jun. 12-15, 2017, pp. 157-160.
- [20] J. Janssen, M. Heijningen, K. Hilton, J. Maclean, D. Wallis, J. Powell, M. Uren, T. Martin, F. Vliet, X-band GaN SPDT MMIC with over 25 watt linear power handling,

- in Microwave Integrated Circuits Conference, 2008. EuMIC 2008. European, pp. 190-193, Oct 2008.
- [201] S. Masuda, M. Yamada, Y. Kamada, T. Ohki, K. Makiyama, N. Okamoto, K. Imanishi, T. Kikkawa, and H. Shigematsu, GaN singlechip transceiver frontend MMIC for X-band applications, in Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International, pp. 1-3, June 2012
- [22] A. Bettidi, A. Cetronio, M. Dominicis, G. Giolo, C. Lanzieri, . Manna, M. Peroni, C. Proietti, and P. Romanini, High power GaN-HEMT microwave switches for X-band and wideband applications, in Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE, pp. 329-332, June 2008.
- [23] S. Osmanoglu, X-band low phase noise MMIC VCO & high power MMIC SPDT design, M.Sc. dissertation, Dep. Elect. Eng, Bilkent Univ., 2014.
- [24] W. Ciccognani, M. Dominicis, M. Ferrari, E. Limiti, M. Peroni, and P. Romanini, High-power monolithic AlGaIn/GaN HEMT switch for X-band applications, Electronics Letter, vol.44, pp. 911-912, Jul. 2008
- [25] V. Alleva, et. al., High power microstrip GaN-HEMT switches for microwave applications, Microwave Integrated Circuits Conference, pp. 194-197, Oct. 2008.
- [26] A. Bentini, D. Palombini and D. Rampazzo, "GaN MMIC SPDTs for C-Ku band beam forming networks applications," 2017 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, 2017, pp. 125-128.