Black Box Model of Integrated Circuits for ESD Behavioral Simulation and Industrial Application Case

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Abstract

In order to design electronic products for Electro Static Discharges constraints, the use of simulation is fundamental. This is the only solution to justify the design and to manage properly the margin during the development. In order to do so, models are required and especially for the integrated circuits (IC). A Pspice model had been developed and validated for ESD performance prediction of IC implemented inside an electronic product. Nevertheless, the practical implementation of these modeling techniques for IC induced some issues, especially under Pspice, being the targeted tool for our simulation. Divergences issues during time domain simulation were frequently observed and sometimes irresolvable with model proposed in [1]. We propose in this article new implementation techniques in Pspice. A practical example is used to demonstrate the capability of our model.

1. Introduction

Electrostatic Discharge (ESD) is a major constraint for electronic product design and especially in automotive domain, where requirements can reach levels up to 25 kV. The reference standard cited in most of carmakers specification is the ISO 10605 [2]. Historically product design was mainly based on experience and experiments, but recent works started to develop modeling and simulation capabilities to justify the design, such as [3,4,5].

The ESD model for IC proposed by various authors, such as [3,4,5], is composed by two main parts. The aim of the first one is to reproduce the electrical behavior of the IC, allowing to obtain correct current and voltage time domain induced at the input of the IC when submitted to transients pulses, and in particular ESD pulses. The second part of the model allows to state on its robustness. In order to generate a model, input information are required. Considering the IC as a black box, the required data for modeling need to be obtained by experimental characterization techniques. These aspects, related to experiment characterization and to the model general structure will be explained in Part II of this paper.

Section II will remind the basic of model generation and will highlights the difficulties for model implementation in Pspice. Section III will introduce two new alternatives methods which will be discussed and analyzed. Section IV will then detail an application example for a SmartMOS component. Finally in conclusion we will propose a synthesis generic modeling approach based on previous works and updated up to our return on experience.

2. Model structure and characterization

In this part we describe the model structure and the techniques / methodology to obtain the data allowing to generate the model.

2.1. General model structure

To understand and introduce our model structure, we need to focus on the typical structure of an IC input (or an output). The IBIS Model [6] provides a good vision of a component structure, as illustrated on Fig.1, and will be used to discuss how these elements influence a pulse waveform applied on such an input.
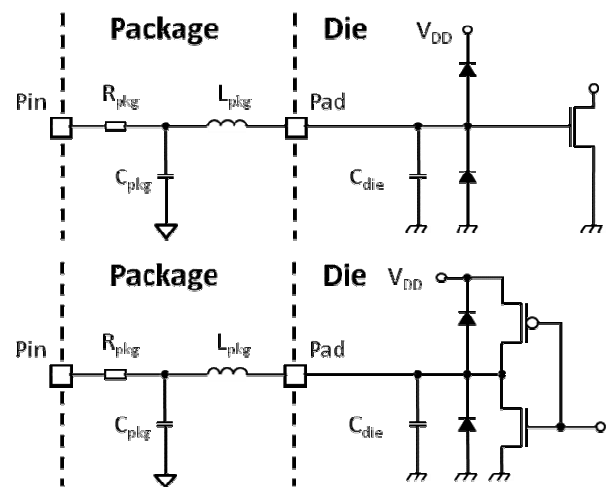

Figure 1: IBIS general structure of a digital Input / Output

The first aspect we need to consider is that an ESD pulse, as defined in [2], has an associated significant spectrum going up to 1 GHz. Even if the considered spectrum in most of references such as [7] is considered until several GHz, we estimate that the most significant part of the energy which could induce a destruction is included below 1 GHz. Disturbances behavior reported in [7] are concerned by this upper spectrum part, but for the focus of this paper, 1 GHz limitation is consistent with the need to analyze only the failure mechanism.

1 GHz is already a quite high frequency, at which any interconnection influence cannot be neglected. As illustrated on Fig.1, IBIS already considered this, since package and bonding wires induce such parasitic elements. These structure elements induce in particular some parasitic inductances (about few nH) which can impact the pulse waveform. These same structure elements also induce some parasitic capacitance that we will have also to consider in our model.

The second important part constituting an I/O structure consists in the internal ESD protection of the IC. It is represented as diodes on the IBIS model general structure of Fig.1. In practice these ESD protections structure can be more complex than simple diodes. Typically ggNMOS structure for example are generally implemented [8]. Whereas IBIS only consider the behavioral modeling of these elements up to 2 times the power supply nominal voltage, ESD generator characteristics lead us to consider a quite larger bandwidth. The aim of these protection elements is basically to shorten the input to the ground (or power supply) in order to derive the pulse energy, and to protect the IC circuitry. To have an idea about the voltage and current sustained by such a protection, we can simply assimilate a protection structure as an equivalent linear resistor. Typical value is about few Ohms (depending on the structure). Based on this typical value we can perform a first simulation by using the ESD generator model, such as the one developed in [9] to estimate the current and voltage seen by the IC during such a pulse.

Fig.2 provides a simulation result for a 8 kV contact discharge on a 2 Ohms resistor, with a 330 pF / 2 kOhm configuration for the generator. This allows to define a global need in the current / voltage range we need to consider for the characterization and modeling. Current up to 30 A in the protection will then be the key targeted value considered. On such a range, the I/V behavior which can be observed, correspond to the ones of Fig.3. Most of embedded ESD protection structures in IC have the particular behavior depicted on left figure of Fig.3. This makes appear what is called a snapback. For low voltage the current is also low and the protection I/V behavior is globally following a linear behavior (pure resistor). As soon as the voltage reaches a certain level (trigger), the protection is activated and creates this snapback phenomenon.
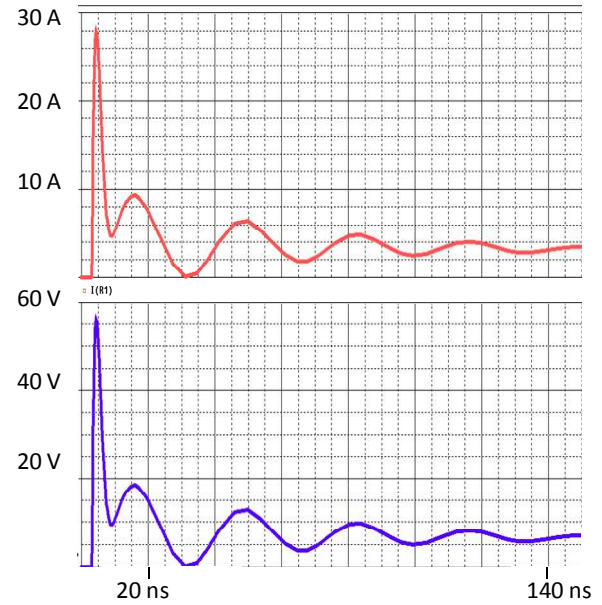

Figure 2: Simulation of induced current and voltage on a 2 Ohms load by 8 kV ESD pulse (2 kOhms / 330 pF).
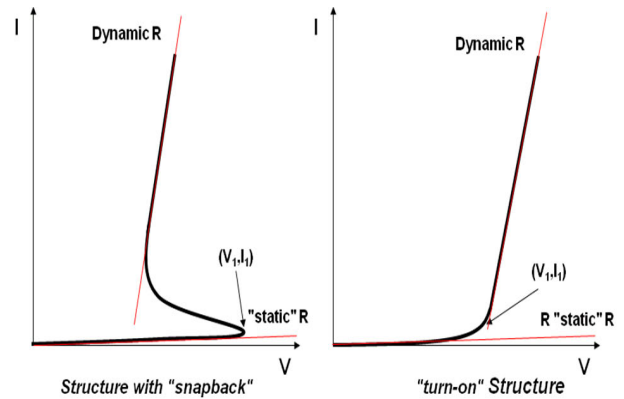

Figure 3: Representative I/V observed on IC input.

After the protection is turned on, it imposes an equivalent resistance value around few Ohms (or even less) depending on its design. We are then is what is identified to be the "Dynamic R" on Fig. 3. The turn on behavior depicted on Fig.3 corresponds to a simple diode structure behavior.

In practice the current won't increase infinitely on the I/V characteristics of Fig.3, and a discontinuity will appear in these characteristics. This happens when the IC is destroyed (breakdown). Either an open circuit or a short circuit will then be created by this failure. Due to the ESD pulse, the internal ESD protection sees important current and voltage values. Depending on the protection design it might be destroyed by one or the other of these electrical characteristic. In case of this is the current which is at the origin of the failure, we can state that the failure mechanism is due to thermal effect. In this situation, the relevant electrical parameter at the origin of the failure is simply the energy value, as introduced and considered in [10]. Another situation might appear, where this is the voltage which

induces the failure. Due to high voltage value, we can reach the dielectric breakdown voltage and induces a spark inside the IC. In this second situation, the voltage threshold value will be the relevant parameter to describe the failure mechanism.

Based on these descriptions and identification of the relevant parameters and mechanism involved during an ESD pulse, we established the general model structure proposed in Fig. 4. This model is composed by 3 parts:

- The PDN (Passive Distribution Network): This part simply consists in the passive elements models related to the package, parasitic capacitor of the ESD protection and functional input impedance.
- The DN (Dynamic Network): This part represents the non linear I/V characteristic of the embedded ESD protection.
- The FB (Failure Behavioral): This part provides the relevant information about the failure mechanism (maximum energy value and/or maximum voltage value sustained).
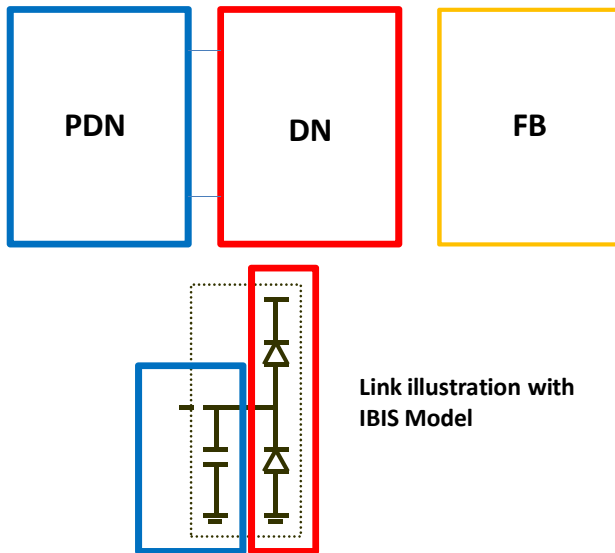

Figure 4: Generic structure of the model proposed.

In the following sections we will describe more about these fundamental blocks and especially how to derive these data from measurements.

2.2. PDN Extraction

In order to extract the PDN the measurements are generally performed with VNA (Vector Network Analyzer). This measurement is then performed with a low level signal, allowing to measure the impedance without the non linear elements activated. This kind of measurement is quite similar to the one performed to generate ICEM-CE [11] or ICIM-CI [12] model. After calibration in the reference plane corresponding to the IC input to be measured, the impedance can be extracted on the frequency range of interest (up to 1

GHz). Taking care about the measurement setup choice to have acceptable uncertainties [13] the impedance magnitude is then obtained. An example of typical measurement result is provided on Fig. 5.
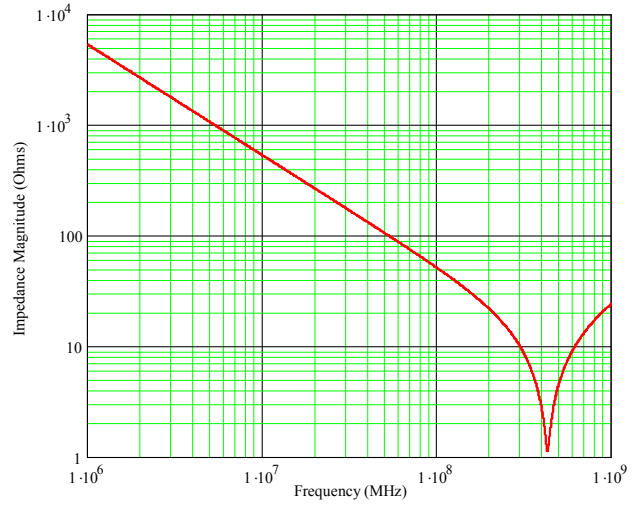

Figure 5: Typical impedance observed from IC input.

From the part of this curve, where the impedance decreases with a -20 dB/decade slope, the capacitance value can be extracted. It corresponds to the global parasitic capacitance related to the package, to the one of the ESD protection elements and of the input circuitry.

From the part of this curve where the impedance increases with a +20 dB/decade slope, the inductance value can be calculated. This one as discussed previously is mainly due to the package and bonding wires.

Finally at the resonance a resistor value can be extracted but mustn't be considered in the PDN construction, this information being implicitly integrated in the DN part of the model. Furthermore, the resistor value we extract here is not appropriate, since it doesn't represent the low frequency resistor value and suffers from the skin effect influence. This resistor and its frequency dependency could be considered and implemented inside the model, based on [14], but based on authors' experience this is not relevant.

2.3. DN Extraction

The DN is no more than the I/V characteristic of the embedded ESD protection in the IC. As discussed previously we need to extract this characteristic up to several tens of Amperes. It is then not possible to obtain these characteristic by applying and making vary DC conditions and another technique had to be considered.

To perform this measurement, we use a TLP (Transmission Line Pulse) generator. This test method is defined in [15] and the basic structure of this generator is depicted on Fig.6. It permits to generate a rectangular pulse, which duration depends on the length of the coaxial cable used. It can be

then possible to generate quite easily pulses with very short durations (10 or 50 ns for example). Up to this characteristic, the energy transmitted to the IC can be minimized and permits to explore the I/V characteristic on the range needed for modeling activity. At the output of the generator we use a 10 dB attenuator allowing to minimize the reflections. Its interest is to simply minimize pulse reflections, to better manage what is transmitted to the IC. It will be of particular interest for the FB extraction detailed in next part. Current and voltage can then be simultaneously obtained by measurements in the quasi static region identified in Fig.7.
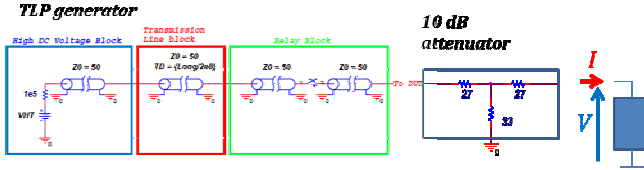

Figure 6: General test setup with TLP generator to perform I/V characteristic measurement.
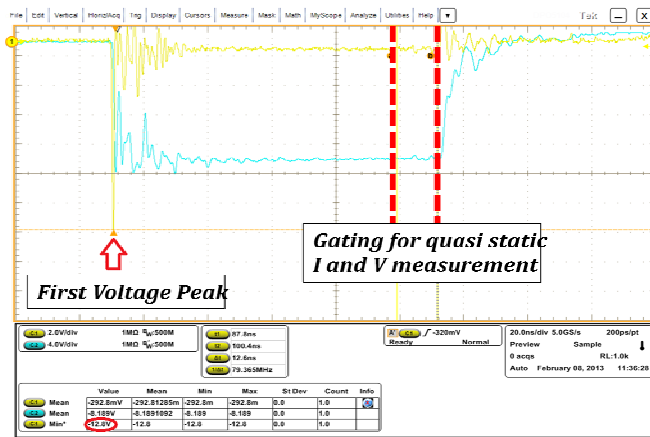

Figure 7: Measurement example.

Increasing the TLP source amplitude progressively allows to build the global I/V characteristic, until the destruction of the device.

2.4. FB Extraction

In order to obtain the FB, we also use the TLP generator according the same setup as the one of Fig. 6. This time we don't focus specifically on the I/V characteristic (even if they need to be measured anyway) and we just determine the level for which the IC is destroyed. This operation can be performed for different pulse length (From 10 ns to 1 μs) and from the result obtained we can determine what is/are the relevant criteria to consider for the FB (energy and/or voltage threshold).

During the TLP injection, we observe a voltage transient at the beginning of the pulse (See Fig. 7). If the component is destroyed because of breakdown voltage mechanism, it will clearly appear in this particular phase. As a consequence

during these characterizations we need to measure for each pulse width the following data:

- The quasi static I and V values at the test level just before the failure (since if the component is destroyed these data can be not relevant anymore)
- The maximum voltage value obtained during the pulse, and generally observed at the beginning of the pulse.

Collecting these data for the different pulse widths, we can plot the energy and the power inducing the failure depending on the pulse width and then proceed to the following analysis to determine the failure mechanism and its threshold value. Generally one of the three behavior depicted on Fig. 8 will be observed.
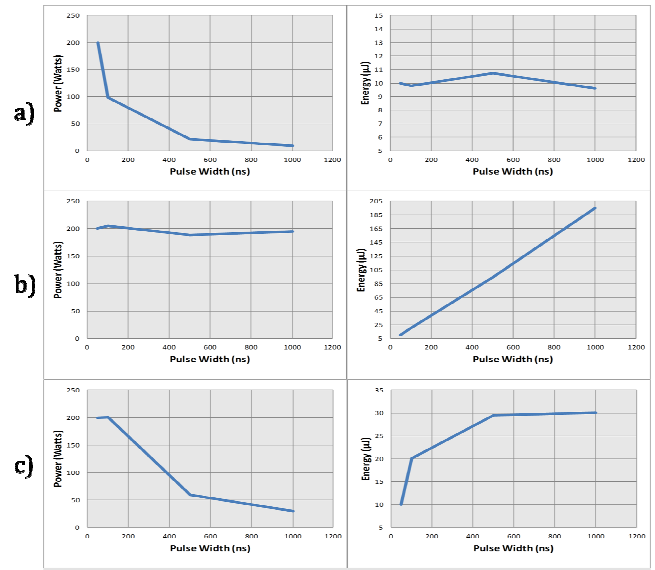

Figure 8: Measurement example.

The first case (Fig. 8.a), Clearly shows the behavior described and justified by [10]. It shows that the energy is globally constant in function of the pulse duration. This means that the component is destroyed because of a thermal mechanism and that this energy threshold value can be used as the FB parameter. In the second case (Fig. 8.b) we observe that the energy is not constant but that power is (Peak voltage amplitude remains constant whatever is the pulse width). This is then representative of a breakdown voltage failure mechanism and the max voltage value inducing the failure will be the FB.

The last situation also commonly observed during these kinds of characterization is the one depicted on Fig. 8.c and corresponding to a mix of the two previous phenomena. For the longer pulses the components is destroyed because of energy. When the pulses are shorter, in order to have the same energy value, voltage and current are for sure increasing, and it can happen that the voltage value increases enough to change of failure mechanism and to have in this area a breakdown voltage mechanism. In such a situation both maximum voltage and maximum energy sustained by the component will be used to describe FB.

Up to the TLP characterization with different pulse widths, it is then possible to determine which failure mechanism is dominating (energy, voltage or a combination of both), and to define the proper value(s) in our model.

In [4], the author focused on energy criteria to develop its model. Whereas good results were obtained, we introduce here a more general approach. We will highlight in part 4 of this article, the importance of differentiating these failure mechanism, especially when looking for design solution to harden a component.

3. Model implementation techniques in Pspice

After describing the methods to collect the required data to be considered to generate a model, we develop in this part the different techniques developed to implement our model in a Pspice environment. Other works, such as [4] or [3] based their models more or less on the same information than the ones described in part 2, but choose different languages or tools for its implementation. What is interesting to note is that all these modeling techniques are based on exactly the same information, and that a standardized model could be defined, by simply defining a clear description method of the PDN, the DN and the FB. The use of XML language could be useful to standardize this model definition, as it has been successfully performed for [11-12] for example.

In Pspice it is quite well known and simple to model the ESD generator, the traces on PCB by using transmission line models and so on. In [13] the association of block models was performed successfully to simulate immunity test method applied on electronic equipment. Most of these blocks are also of concern when dealing about ESD, so in order to take benefit of the existing and developed models, we decided to use Pspice to perform also this kind of analysis.

3.1. State of the art

The first approach developed to implement such a model in Pspice was first introduced in [5]. It consists in considering the V/I characteristic (and not the I/V in order to have a monotonic response, as on Fig. 9). This characteristic is then placed in the model structure of Fig.10. In this model, the H controlled source extract the current in the circuit side. This value is injected in a ETABLE model inside which the V/I table is implemented. The output voltage is then injected back in the circuit part. Between the both a RC filter is generally used to partially manage the Pspice divergence issues. This small low pass RC filter allows smoothing and suppressing unrealistic fast variations in the extracted current value and in the given equivalent resistor value. In the case of Fig.10 this RC is set to have a cut off frequency around 600 MHz (considering that any faster variation is not so physical), and this allows to reduce convergence issues in

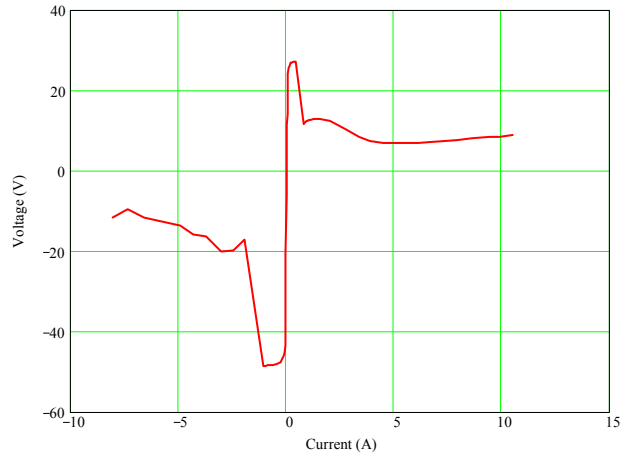Pspice. This model is then completed with the LC values corresponding to the PDN.

Figure 9: Typical V/I characteristic implemented in a Pspice model.
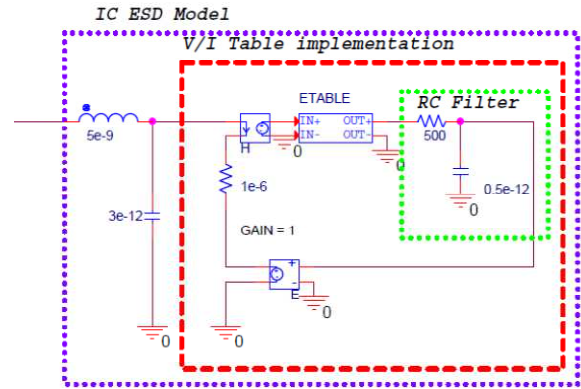

Figure 10: Pspice model suggested in [5]

Whereas this model can theoretically reproduce the electrical behavior of the IC submitted to pulses, divergence issues were frequently observed in time domain simulations (infinite current values, too high current variation between two simulation step time, inducing a mistake and stop of the simulation). A way to minimize this problem was to implement the RC filter already discussed. Due to important discontinuities in this way to describe the device behavior, it leads to this problem and other solutions had to be found. It was also noticed that structures with snapback behavior were even more problematic to be managed with this method.

For the following modeling strategies we only focus on the DN part of the model. The PDN and FB parts remaining the same whatever are the techniques used.

3.2. Diode model structure

This first model we proposed can only be applied on I/V characteristic having no snapback phenomena. The basic

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idea is to use a perfect diode model in Pspice in series with a resistor and with a voltage source (Fig.11).
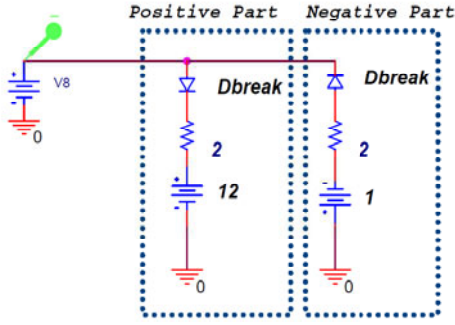

Figure 11: Basic of the "diode" model

One part of the model is dedicated for positive part and the other one for negative part of the I/V characteristic. Turn on value is managed by the voltage source and the dynamic resistor value can be tuned accordingly to the measured data. A basic example is provided on Figure 12.
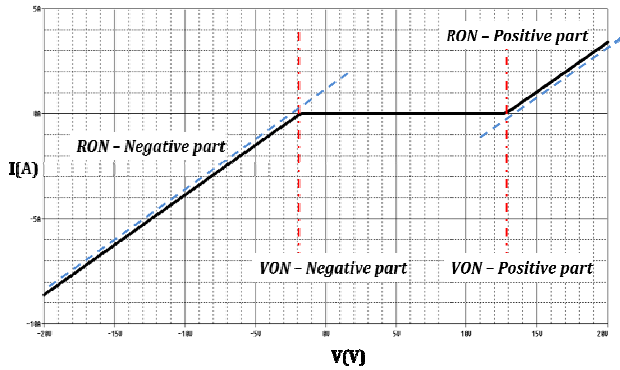

Figure 12: Basic of the "diode" model

Based on this basic structure, we propose to use several of this elementary model, as proposed on Figure 13, in order to create more complex non linear behavior. The interest of this structure is that it can create slope variations in I/V curve, with a very simple unknown identification and implementation in Pspice. Figure 14 shows the characteristic of each branch of the model and the result when combining them. This can be extended to higher number of branches and permit to fit slopes changes that we can observe in practice. This model is quite more robust for time domain simulation since it doesn't generate discontinuities.
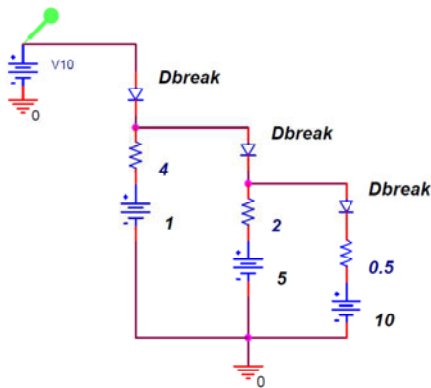

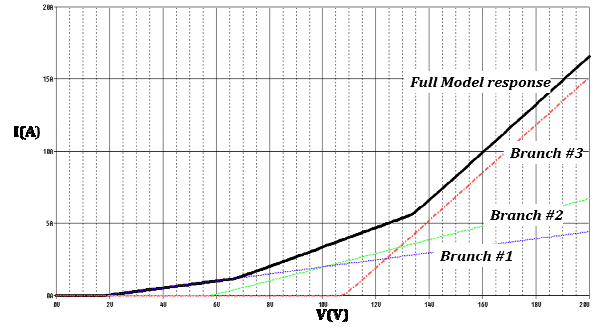Figure 13: Advanced "diode" model typical structure

Figure 14: I/V of advanced "diode" model

Whereas this model is quite robust for time domain simulation, we needed to develop new methods to consider also the snapback phenomena.

3.3. Switch model structure

This second technique is more interesting since it allows to consider particular snapback effects and to be very stable for time domain simulation. It is based on the use of a Pspice elementary switch model. The principle of this elementary model is that it makes vary a resistor with a LOG behavior between two thresholds, as illustrated on Figure 15. On this schematic, the current value is extracted up to H controlled source and drives the switch. On this example, the switch resistor varies between ROFF (1MOhms) and RON (1 Ohm) between current values from 10 mA to 80 mA.
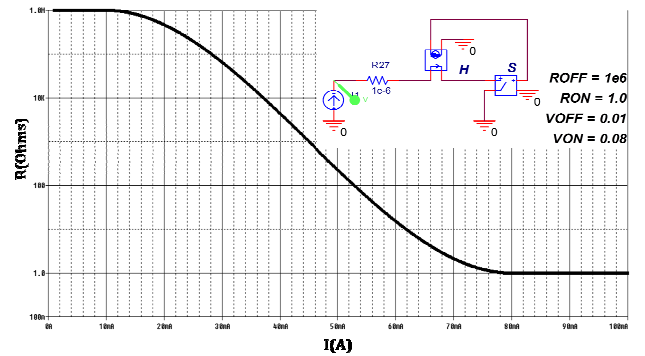

Figure 15: Resistor behavior of the "S" switch model between two defined thresholds values.

Then instead of producing a I/V (or V/I) characteristic we need to focus on R(I) characteristic. An example, corresponding to the application case discussed in section 4 is provided in Figure 16. We can observe an interesting behavior where the resistor value only decreases when the current increases and that depending on the decreasing slope this can make appear or not a snapback phenomenon. This R(I) characteristic corresponds to the I/V one provided on Fig.18 and clearly making appear a strong snapback effect.
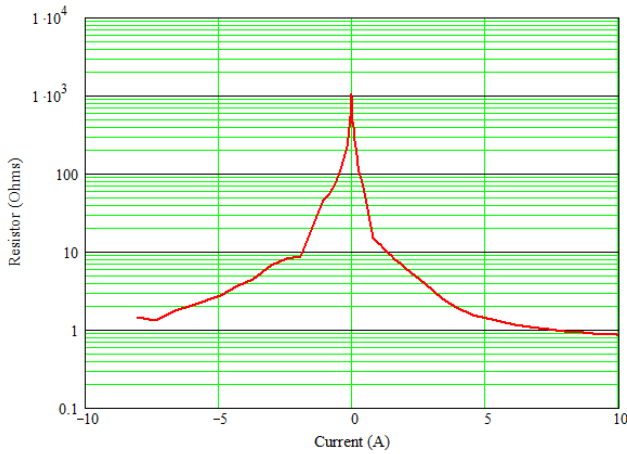
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Figure 16: Typical R(I) characteristic allowing to reproduce the snapback effect.

Electrically speaking the result is exactly the same, but in the way the model is generated this approach is quite innovative. For the next techniques exposed we will only focus on the positive part of the I/V characteristic, but these techniques can be applied by simple extension for the negative parts without any particular difficulty.

In order to fit with a R(I) curve, one switch won't be enough. It is then possible either to consider several switches placed in series (Fig. 17) or to use several in parallel as it will be discussed later.
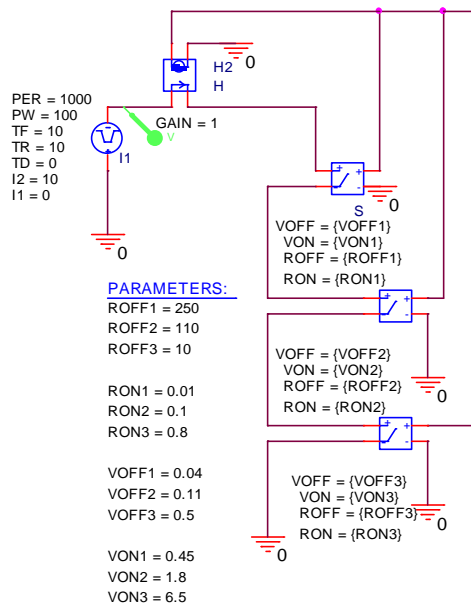

Figure 17: Serial "Switch" model proposal

The R(I) curves obtained with a 3 switches configuration is plotted on Fig. 18 for the particular application that we will introduce in next part. Resulting V/I curve is provided on Fig. 19. The accuracy obtained with only 3 switches is already good, but could anyway be improved with additional ones, by making effective each switch on a smaller current band.
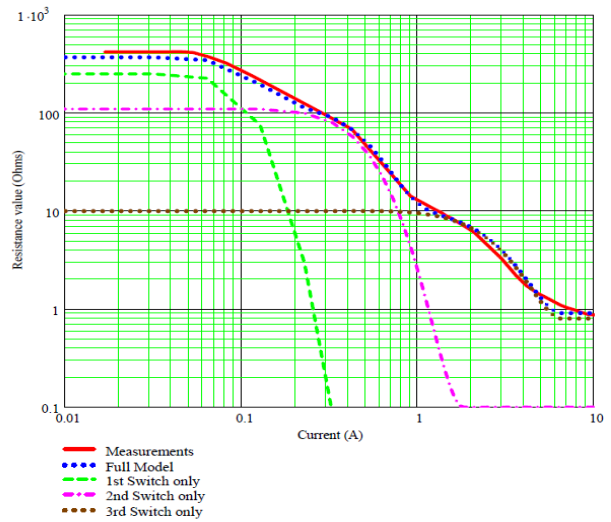

Figure 18: R(I) measured compared to model for model from Fig. 17.

The second approach proposed based on the use of Pspice "S" Switches, consists in placing these switches in parallel this time. The first branch fit the R(I) curve until a certain current value, above which the second branch is activated, while the first one is deactivated. We also use Pspice Switch models to activate and deactivate the branches. The parameters of this activating and deactivating switches are linked for N and N+1 branch to keep the continuity in the global R(I) characteristic.
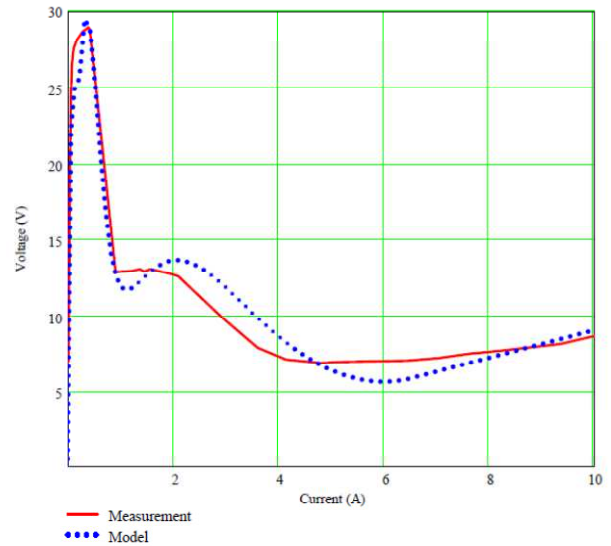

Figure 19: Corresponding V/I characteristic measurement compared to serial "switch model" proposed structure.

An example of such a model also applied for the application developed in next part is given on Fig.20. Resulting R(I) and V/I results are given respectively on Figure 21 and 22.
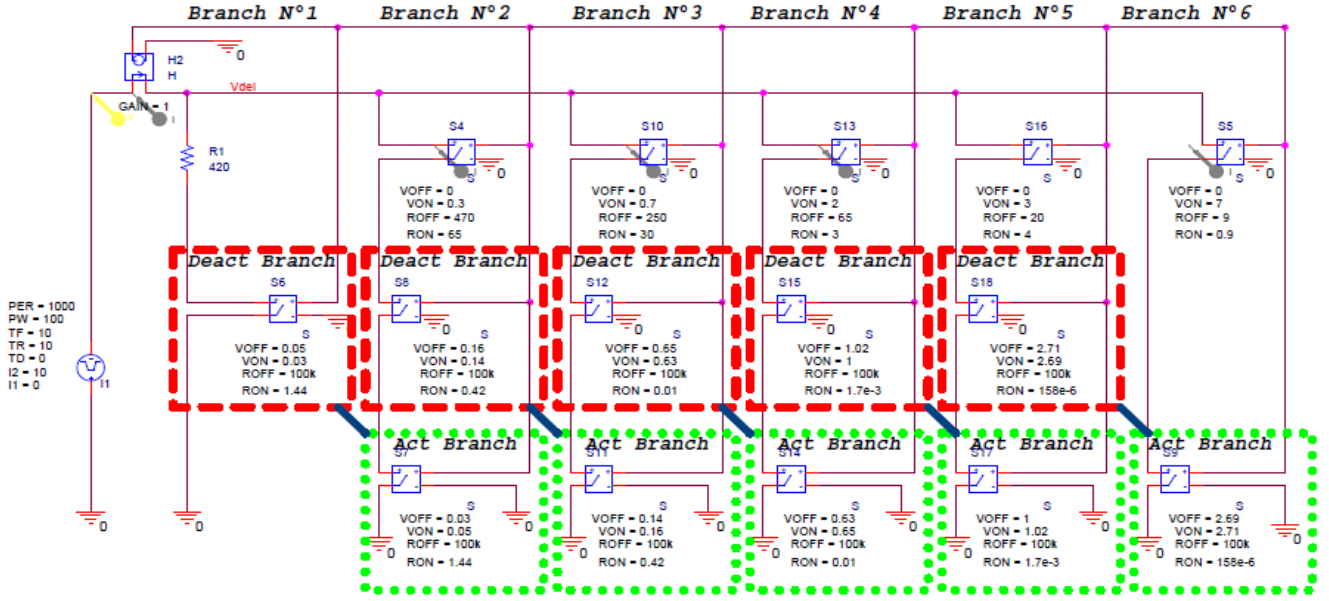
Figure 20: Parallel "Switch" model proposal

This model is also quite stable for transient simulation and has the advantage to be more "simple" to generate, even manually like it is the case for this example. The number of branch is theoretically not limited and would permit to have a better accuracy, even if the results already obtained and given hereafter are quite enough and good to be used for product design and analysis.
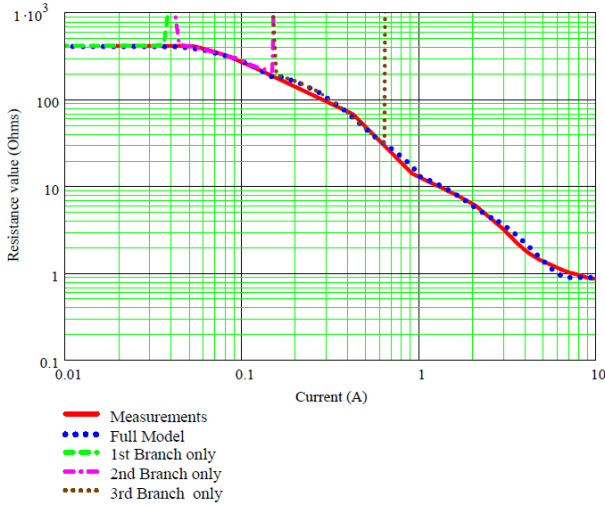

Figure 21: R(I) measured compared to model for model from Fig. 20.

Both proposed model structures allowed to improve the Pspice stability for time domain simulation. The negative point is about the model generation flow complexity. In order to tune properly the number of required switches and to tune properly their parameters, algorithm had to be developed.
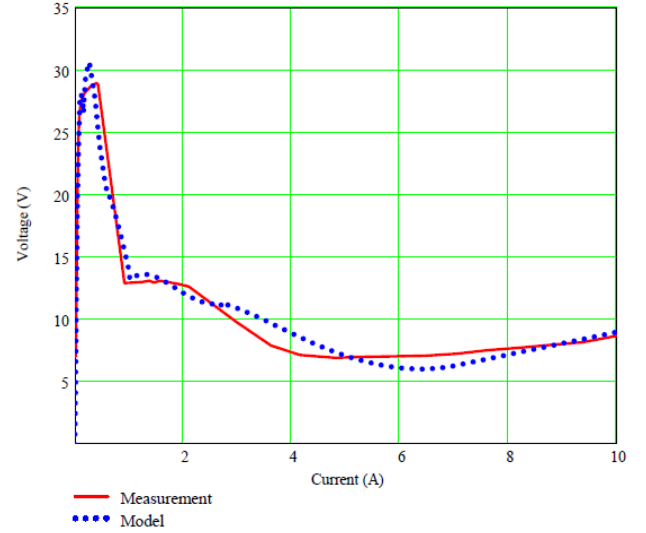

Figure 22: Corresponding V/I characteristic measurement compared to parallel "switch model" proposed structure.

3.4. Dynamic resistor model structure

With the previous modeling approach, we found out that R(I) consideration could be the key to improve the model stability within Pspice. Combining these previous methods reviewed, we propose then a new approach to produce the model. We suggest to use the R(I) characteristic and to implement this characteristic in a ETABLE as shown in the model Fig. 23. This model is quite close in term of structure to the one described in 3.1 but will operate based on the R(I) characteristic as follow: it extracts the current value up the H controlled source. This value is then injected in the ETABLE to extract the resistance relative value which is multiplied by the current value up the MULT operator. The

final value obtained is then the voltage to be injected back on the circuit side with the E controlled source.
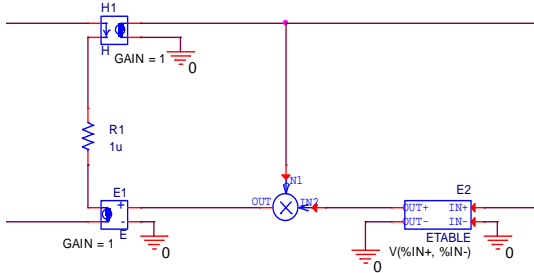

Figure 23: Dynamic resistor model general structure

This model then allows to consider the snapback effect. Stability is then quite improved in Pspice use. Nevertheless, without being able to evaluate it properly the authors identified that the stability is not as good as the switch model.

3.5. Synthesis of models

Based on the models developed in [5] and its detailed improvement exposed in this paper, we can establish a synthesis of their main characteristics (Snapback consideration in the model, stability of the model in simulation and difficulty to produce the model). This synthesis is provided on Table 1.

Table 1: Synthesis of models characteristics and performances.

Model	Snapback	Stability	Production difficulty
ETBALE I/V	Considered	Poor	Very easy
Diode model	Not considered	Excellent	Easy
Switch model	Considered	Good	Difficult
Dynamic Resistor	Considered	Good	Very easy

The stability criteria evaluated in table 1 corresponds to a subjective evaluation by the authors through many simulation applications for ESD or TLP analysis. The difficulty here is that the root causes inducing such instabilities are not well managed or documented in the literature.

Based on this analysis, the Dynamic resistor model can be considered as the best choice / compromise and is currently the final best result that we developed. It has anyway interest to exposed this evolution and describe these behavioral modeling techniques which can be considered in Pspice.

4. Industrial application example

4.1. Application description

A particular application was analyzed up to our modeling strategy. This application is based on the use of a SmartMOS component used to drive Fog lamps on a car. The specificities of such a function is that it drives so much current (with PWM), that the use of serial filtering elements and capacitors values allowed on the line are limited. This can make the ESD hardening a bit tedious.

On the application, exactly the same interface schematic is used for the both fog lamps (right and left side), but between both sides, important differences in ESD robustness were observed on the final application. Make and estimate the difference in this robustness by experiments was difficult due to known repeatability issues with ESD tests. Nevertheless, tests on about 30 products had been conduced and allowed to make in evidence a clear difference in the robustness (about 50%). We wanted, up to the simulation, to identify the influent parameters and explain these differences.

4.2. Model production

The model had been extracted for this component as detailed in section 2. The I/V characteristic was extracted with a 50 ns pulse duration, and corresponds to the one provided already on Fig.9. The DN part of the model was based on the switch models structures as described in section 3.3.

During the characterization to obtain the FB part of the model, we clearly made in evidence that the energy didn't seem to be the relevant criteria, since it wasn't constant depending on the pulse duration (these results are summarized in table 2). As discussed in section 2.4, fundamentally an IC can be destroyed either by thermal effect or by overvoltage, and it seems that in our case we faced this particular second situation, since the peak amplitude remains globally constant depending on the pulse duration (around 225 Volts). This voltage threshold will then be used as the failure criteria to complete our model and for further analysis.

Table 2: Synthesis of models characteristics and performances.

Test #	Pulse width (ns)	Quasi static current (A)	Quasi static Voltage (Volts)	Peak Voltage (Volts)	Calculated energy (µJ)
1	100	12.7	11.3	225	14
2	500	11.7	12	220	70
3	1000	12.2	8.8	230	107

This concrete example is a demonstration that the voltage failure mechanism is also relevant to be considered in a general modeling process. It was not considered in [4], and the model structure we proposed here is then more general.

4.3. Analysis

The fact that the device is destroyed by an overvoltage mechanism makes the things quite different in the protection design. Usually when such a function fails during ESD test, one try to increase the protection capacitors values placed at the input, from 10 nF to 22, 47 and even 100 nF. In experiments such a solution surprisingly didn't work. We wanted then to use our model to make in evidence and understand the reason of such an observation.

The results provided on Figure 23 correspond to simulation of the voltage at the IC input for a 15 kV ESD pulse applied on the IC and with 10, 22 and 100 nF capacitor protection mounted.
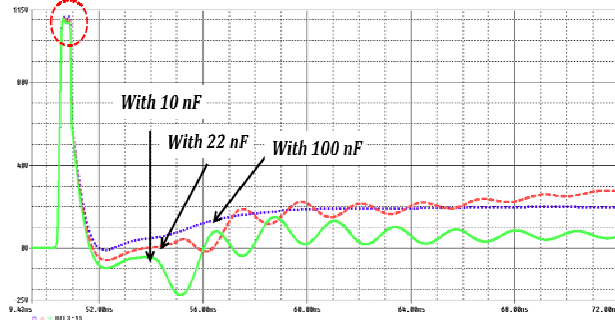

Figure 23: Voltage at IC input during 15 kV ESD pulse applied on IC with 10, 22 or 100 nF capacitor protection.

The Peak voltage is similar for these 3 configurations, and is about 110 Volts. This voltage is imposed by the parasitic inductance of the capacitors themselves, which are globally the same whatever is the value (parasitic inductance of the package being about 1 nH). A parametric simulation on this inductance value clearly makes appear that it impacts this first peak amplitude.

So even if the energy decreases up to this change of capacitor value, the robustness is not changed, since the first peak amplitude remains constant. We can then understand and justify what happened during experiment. Considering that simulation time for such an analysis is only about few ten seconds it also makes in evidence the high interest of simulation to perform this analysis.

At this step we can then focus on the analysis regarding the robustness difference between left and right side. The layout analysis makes appear a difference in the connection length of the capacitors between left and right side. For the right side, state of the art is applied, with the capacitor directly on the path of the trace, and with short connection length to go to the ground. As we can observe on the Figure 24, the

layout of the left side is not in the same situation. The capacitors are not placed on the direct trace, but a dedicated trace is used on the bottom side to connect them. This induces a parasitic additional inductance in series with the capacitors. Based on the length of this traces the additional inductor value is roughly estimated at 4 nH, by using the general 1 nH/mm rule of thumb.
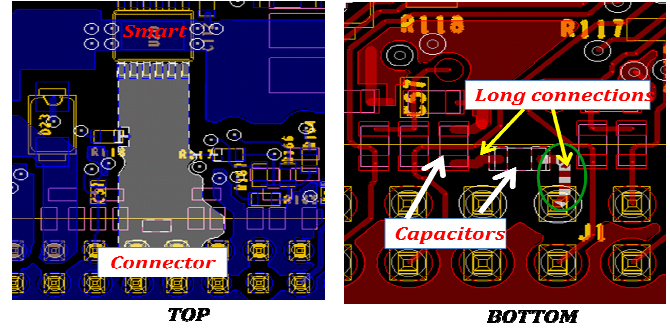

Figure 24: Layout description of the left side.

The simulation results for 15 kV ESD for the induced voltage at the IC input are provided on Figure 25. This makes in evidence that because of this additional parasitic inductance the peak voltage is multiplied by a factor 2 between left side and right side. The robustness is then divided consequently by the same factor 2. Simulation with 15 kV shows on this left side that the robustness cannot be guaranteed, since the peak level is identified at 230 Volts, compared to the FB value we specified at 225 Volts.
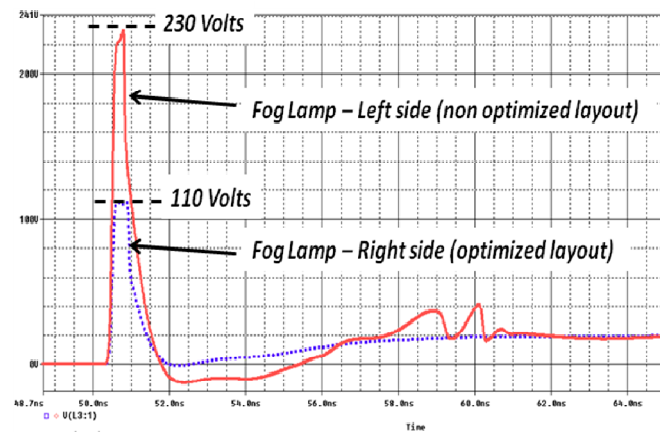

Figure 25: Voltage induced during ESD pulse on left Vs right side

The results and observations made on this application are well reproduced up to the model we developed. By simulation, and up to the availability of such a model, we can estimate directly during the design if a layout strategy or definition is appropriate or not.

5. Conclusions

This paper exposed the structure of a model as well as methods for its integration in Pspice. This model allows to predict the ESD performances of an IC inside an electronic product. It corresponds to an additional step in this research topic which complete those developed in [3-5].

We improved the stability of the model up to new Pspice model structure proposed, which makes our methodology applicable in an industrial and practical context.

The maturity of this modeling technique reaches an advanced enough level to be seriously considered for a standard proposal in TC47A standardization committee. The content proposal for this standard model will be based on:

- The DN, consisting in the I/V characteristic on a range to be specified in order to cover the ESD levels applied at application levels (as explained a 30A range should be a typical required target for this characteristic).The preferred technique for this extraction could be the TLP method, but it can be envisaged that other techniques would also allow to asses this characteristic (extraction from design in particular).

- The PDN, corresponding to the linear impedance of the IC and mainly related to parasitic elements (capacitance, inductance and eventually resistance). The recommended method to get these values is to use a Network Analyzer or Impedance meter.

- The FB, which in addition to the previous information provides the failure threshold in term of max voltage and/or max energy criteria. These characteristics being also extracted by recommended TLP method.

We suggest that these information could consist in the model described in the standard, using an XML format as for [11-12]. Parser will then have to be developed in order to generate the model, linked to the tool in which it is supposed to be used. In our case the parser will be oriented for Pspice models creation as described in this paper.

Acknowledgements

This model was initially imagined and developed to consider ESD pulse applications. We expect that the use of this model could be extended for other kind of pulses, such as EFT or longer pulses up to several micro seconds characteristic times.

Additional validation should be conducted on these particular aspects in order to delimitate the validity domain of our model. This could be the focus of future works.

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